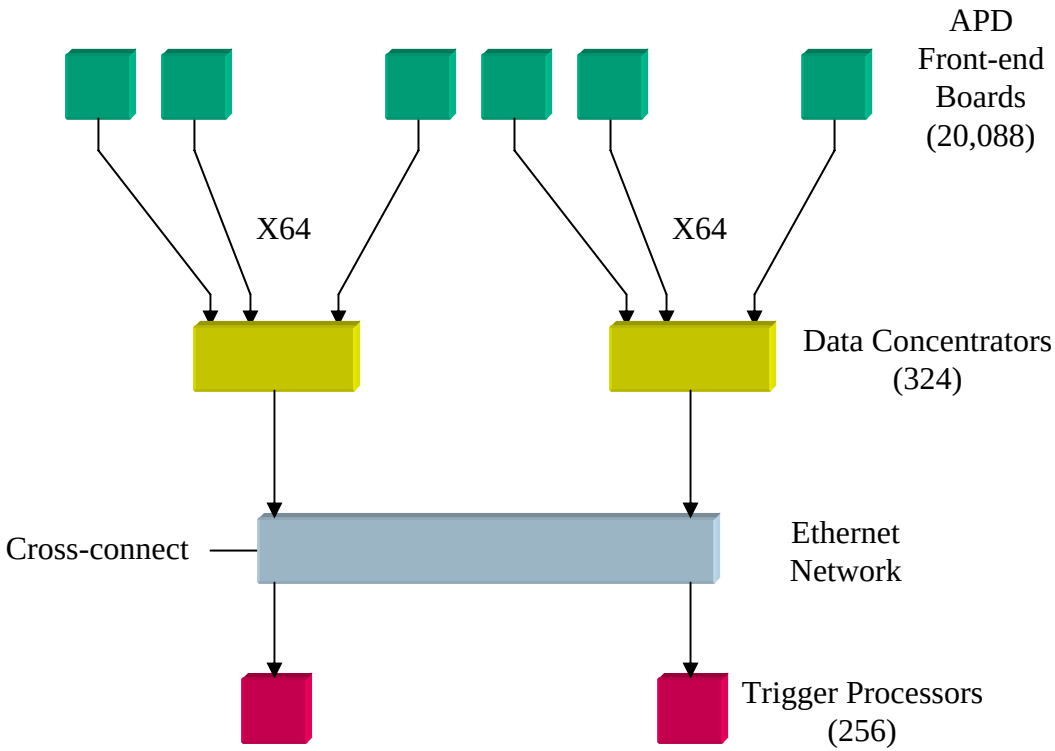
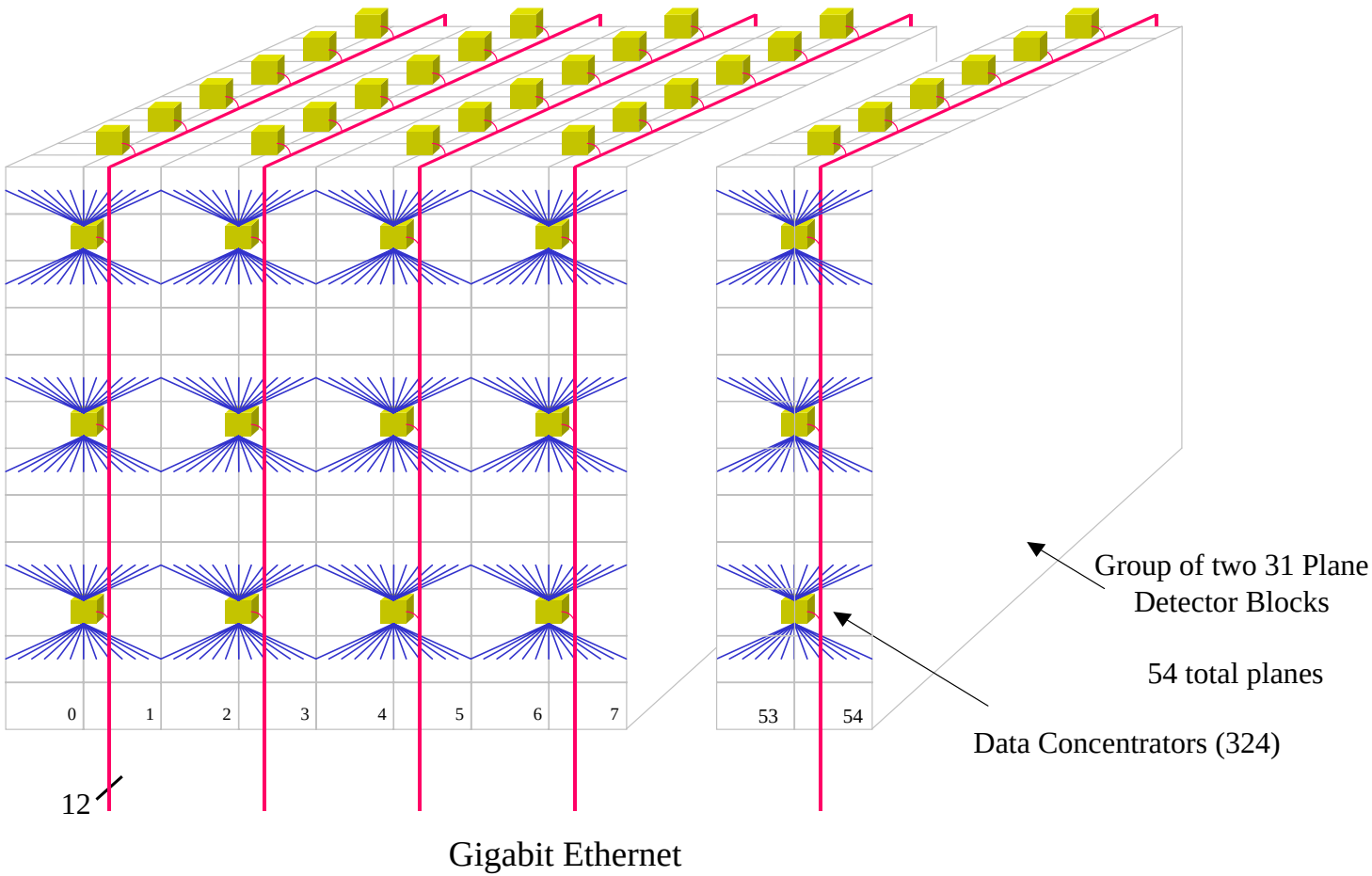
# NOvA DAQ

- 642,816 channels @ 300 hits/sec avg.
- 20,088 Front-End Boards (~ 3 MByte/sec data rate per FEB)
- 324 Data Combiner Modules, each reading out 64 FEBs.
- 1.8 to 3.5 GByte/sec detector data rate.

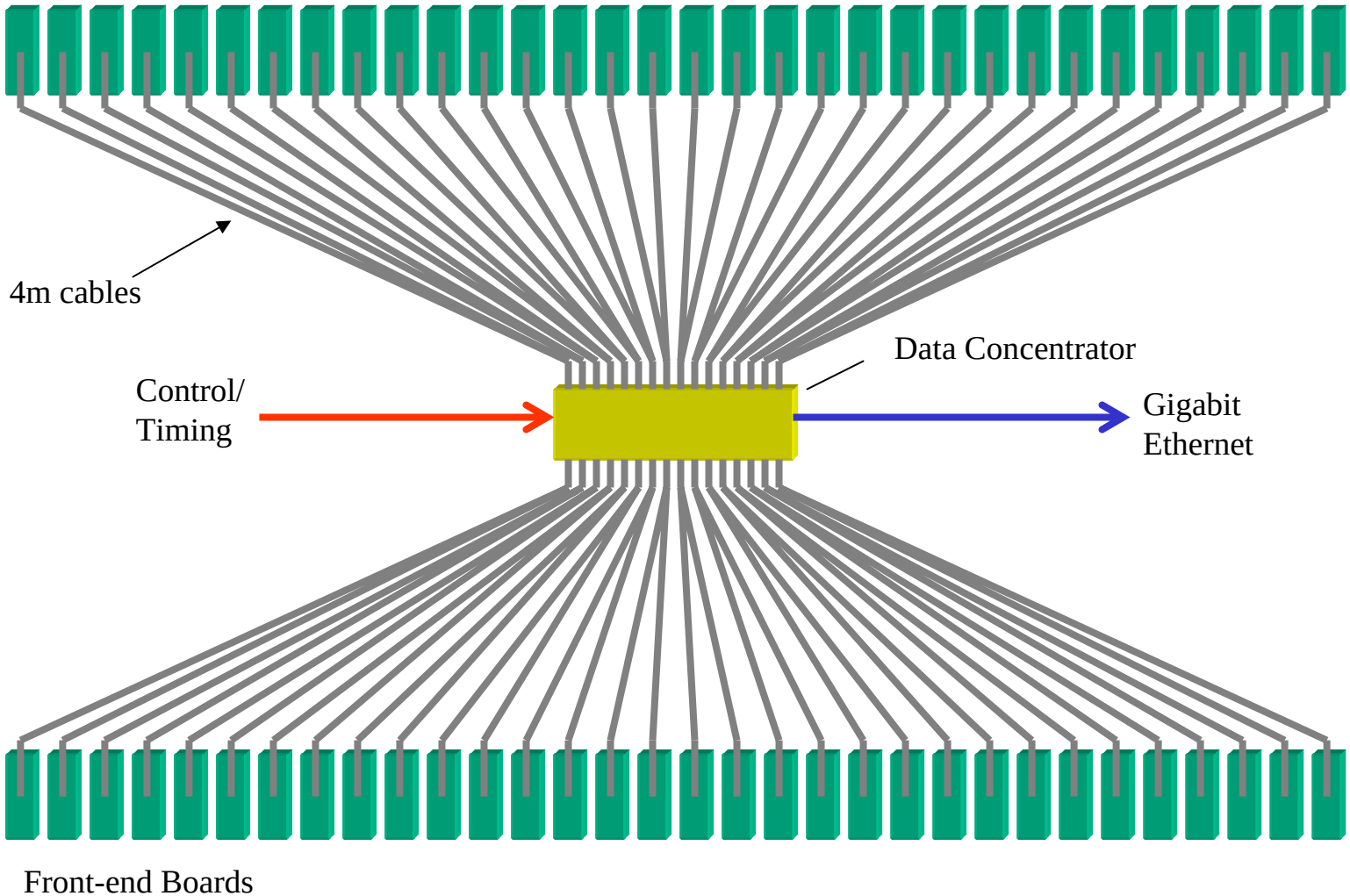
# DAQ - 1.7.x and 2.7.x Front-end Data to Farm



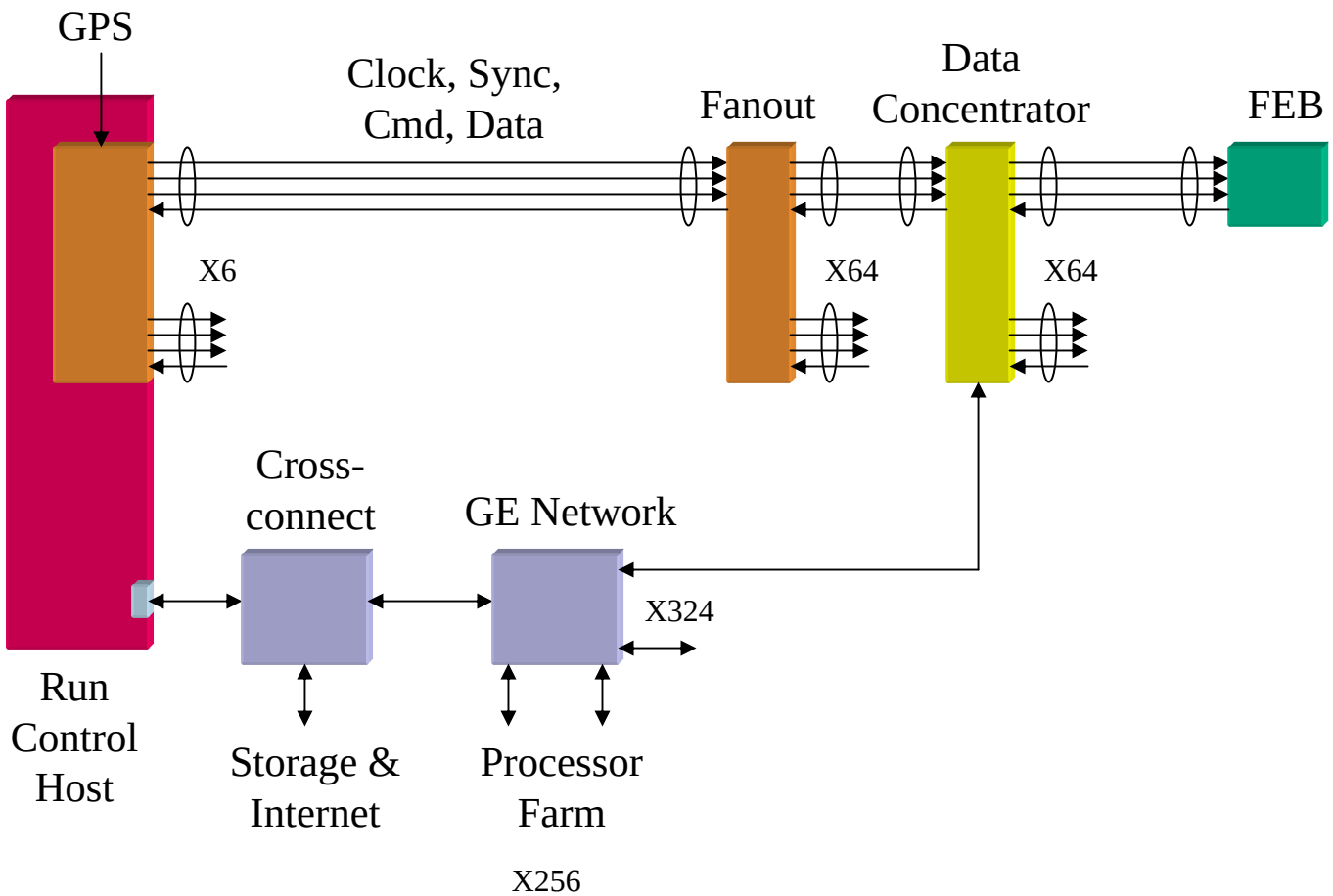
# DAQ on the Detector



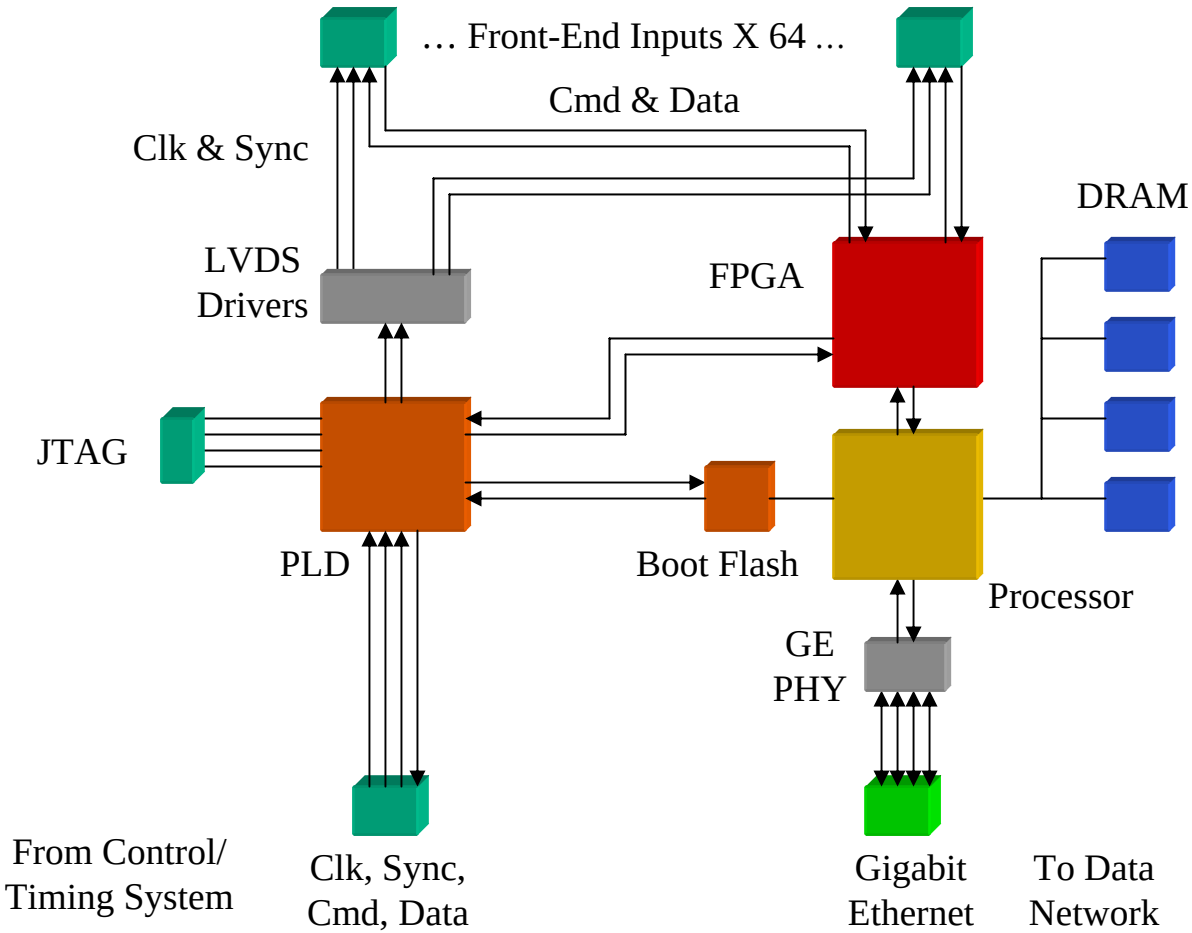
# DAQ Network


4m cables
Data Concentrator
Control/
Timing
Gigabit
Ethernet
Front-end Boards

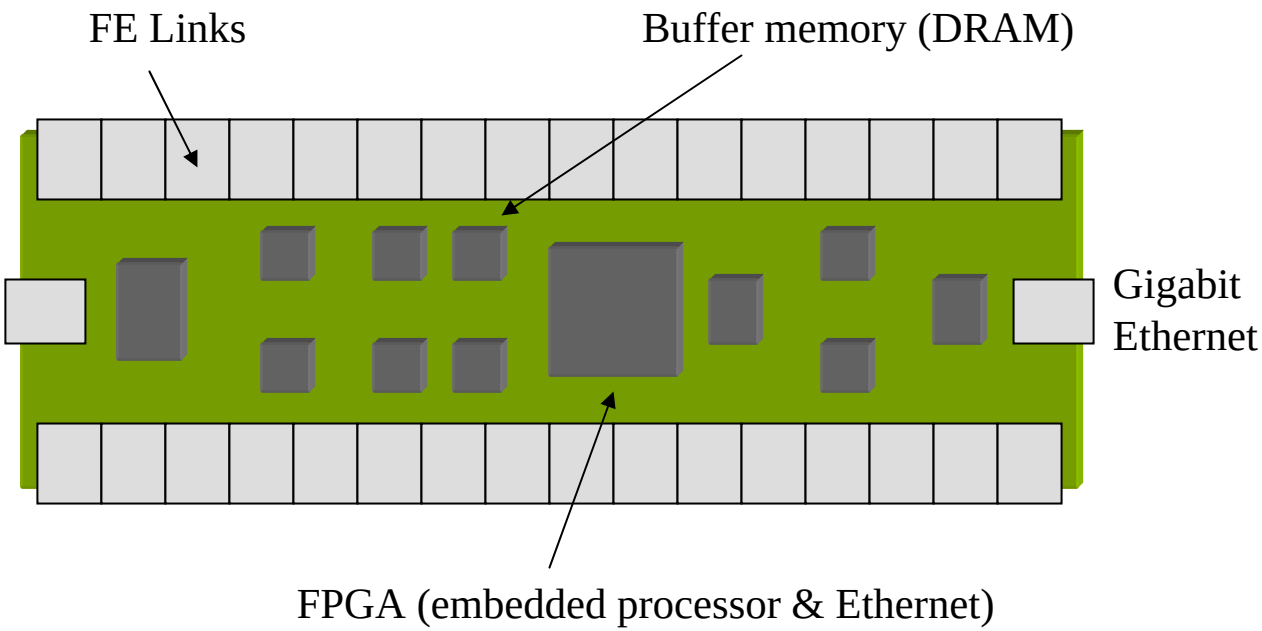
# Timing System



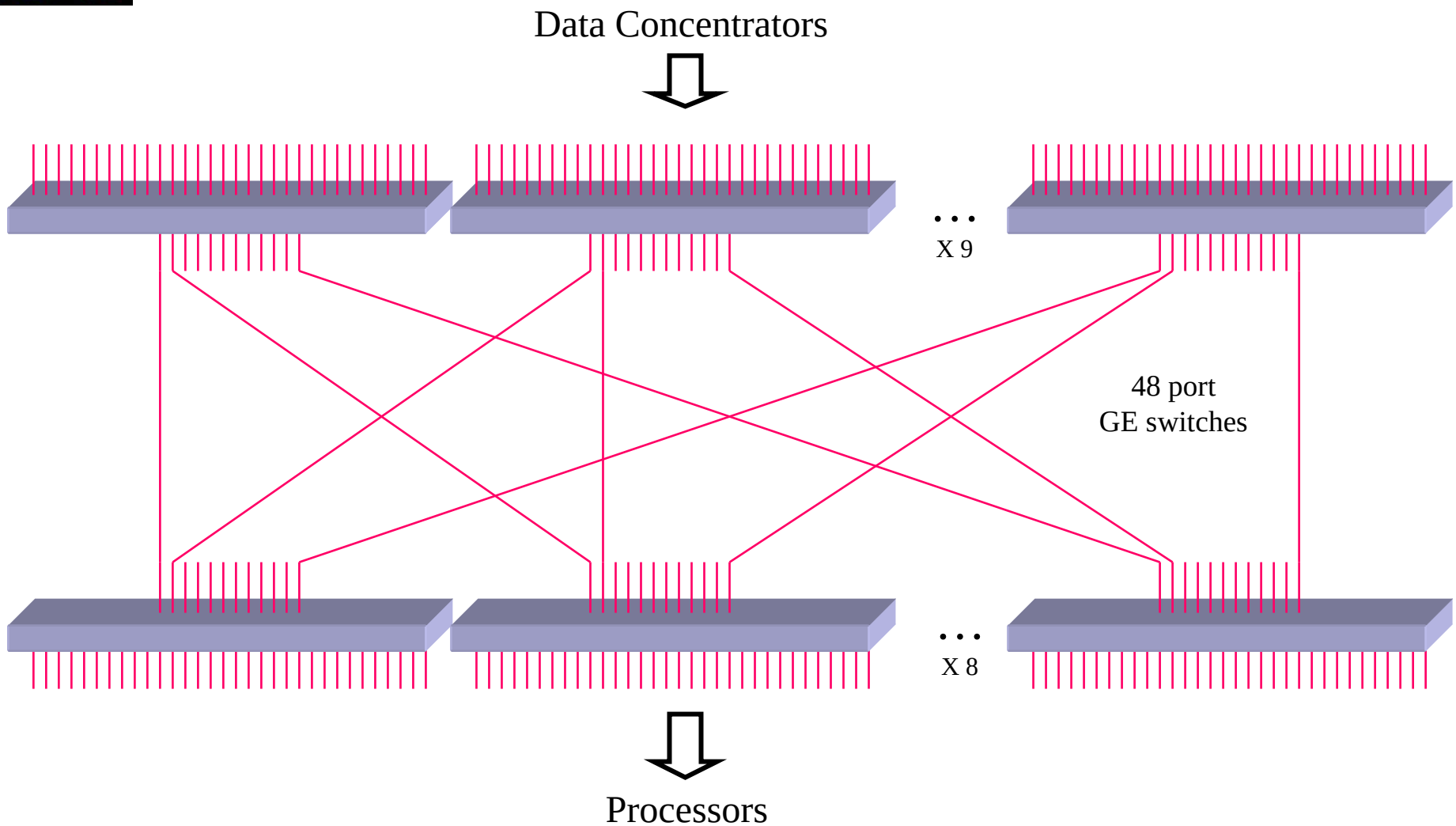
# DCM Block Diagram



# DCM Layout


FE Links
Buffer memory (DRAM)
Gigabit
Ethernet
FPGA (embedded processor & Ethernet)

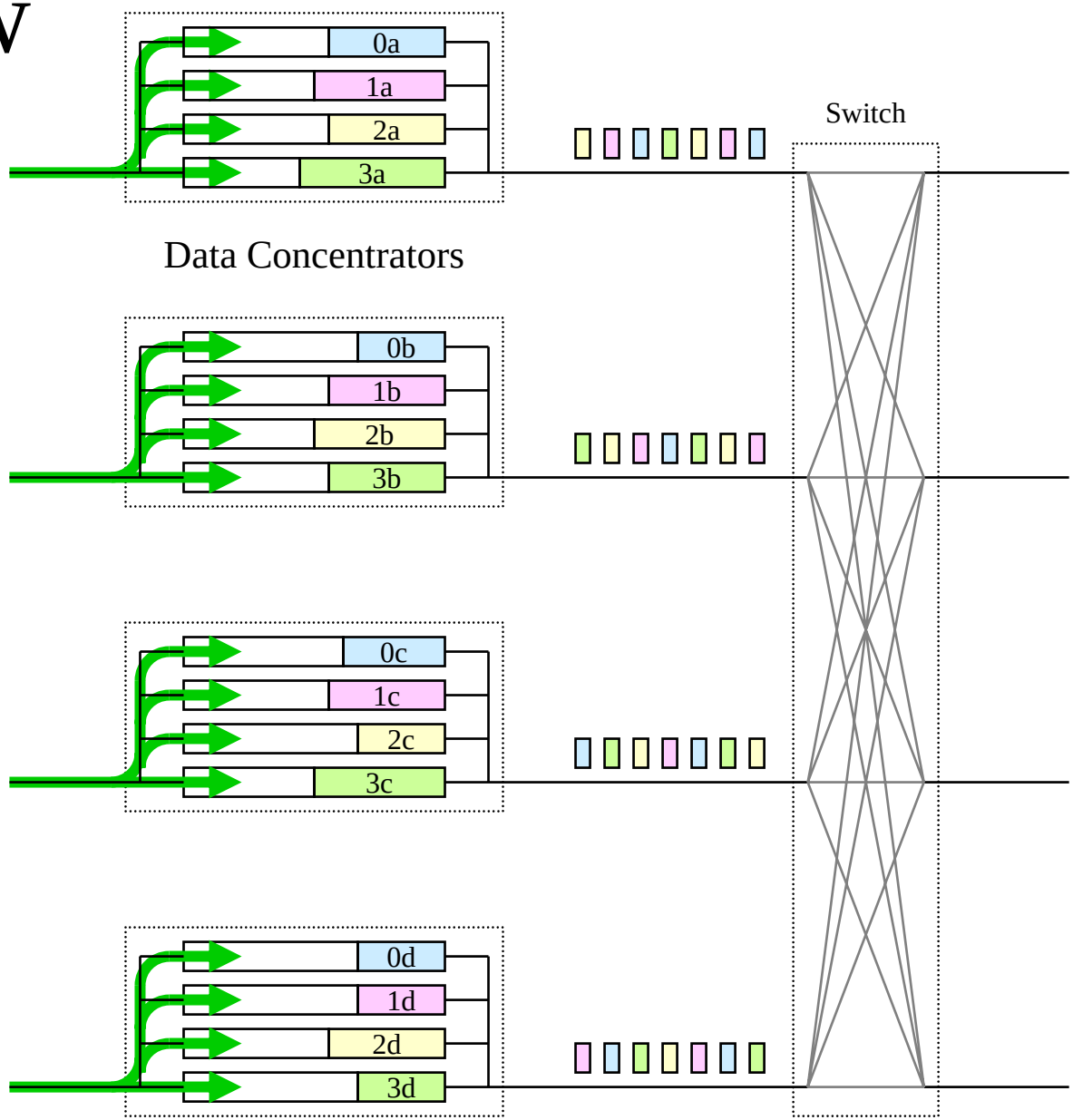
# DAQ Network



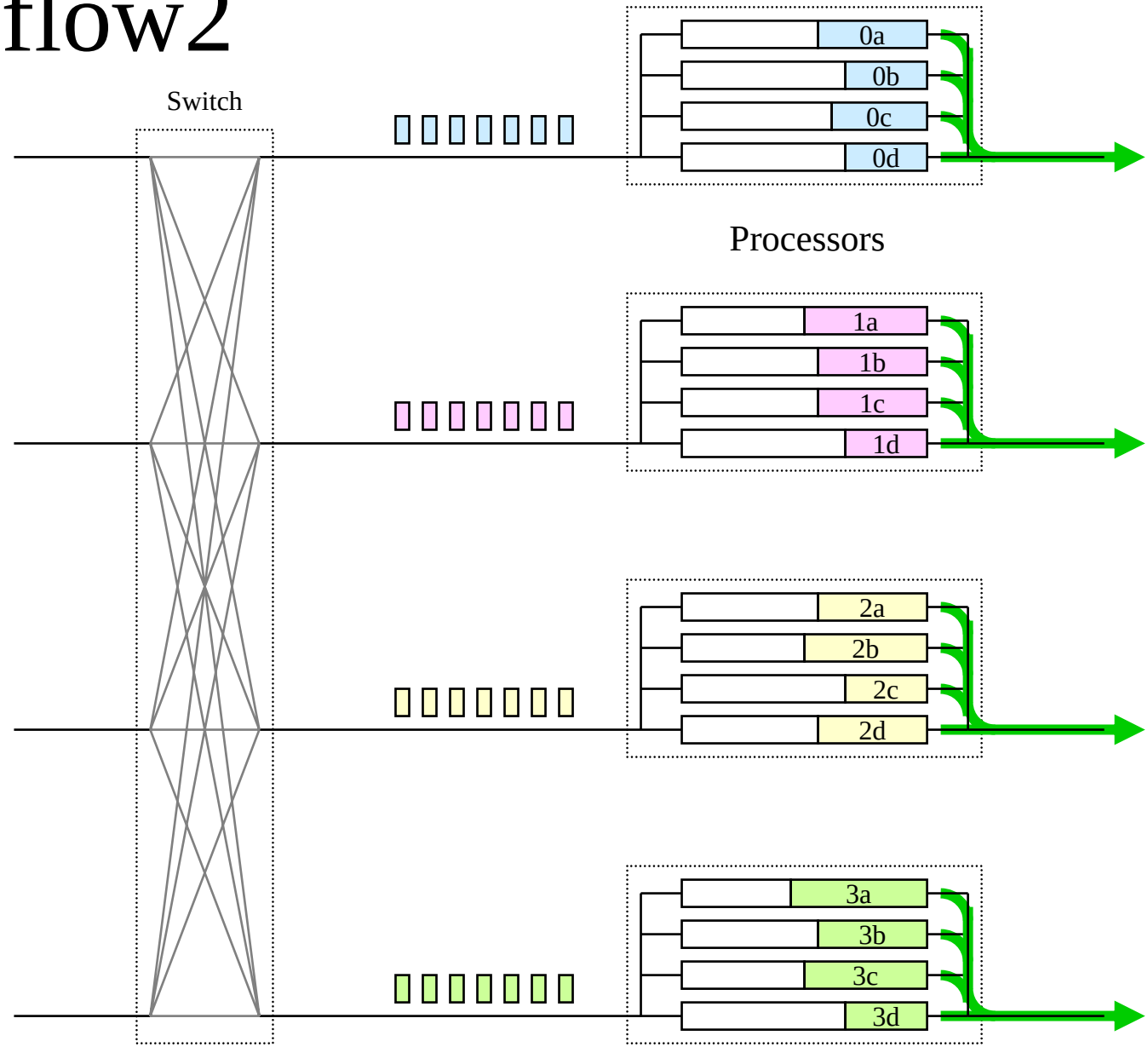
# DAQ Network - Realization

**COTS SWITCHES**

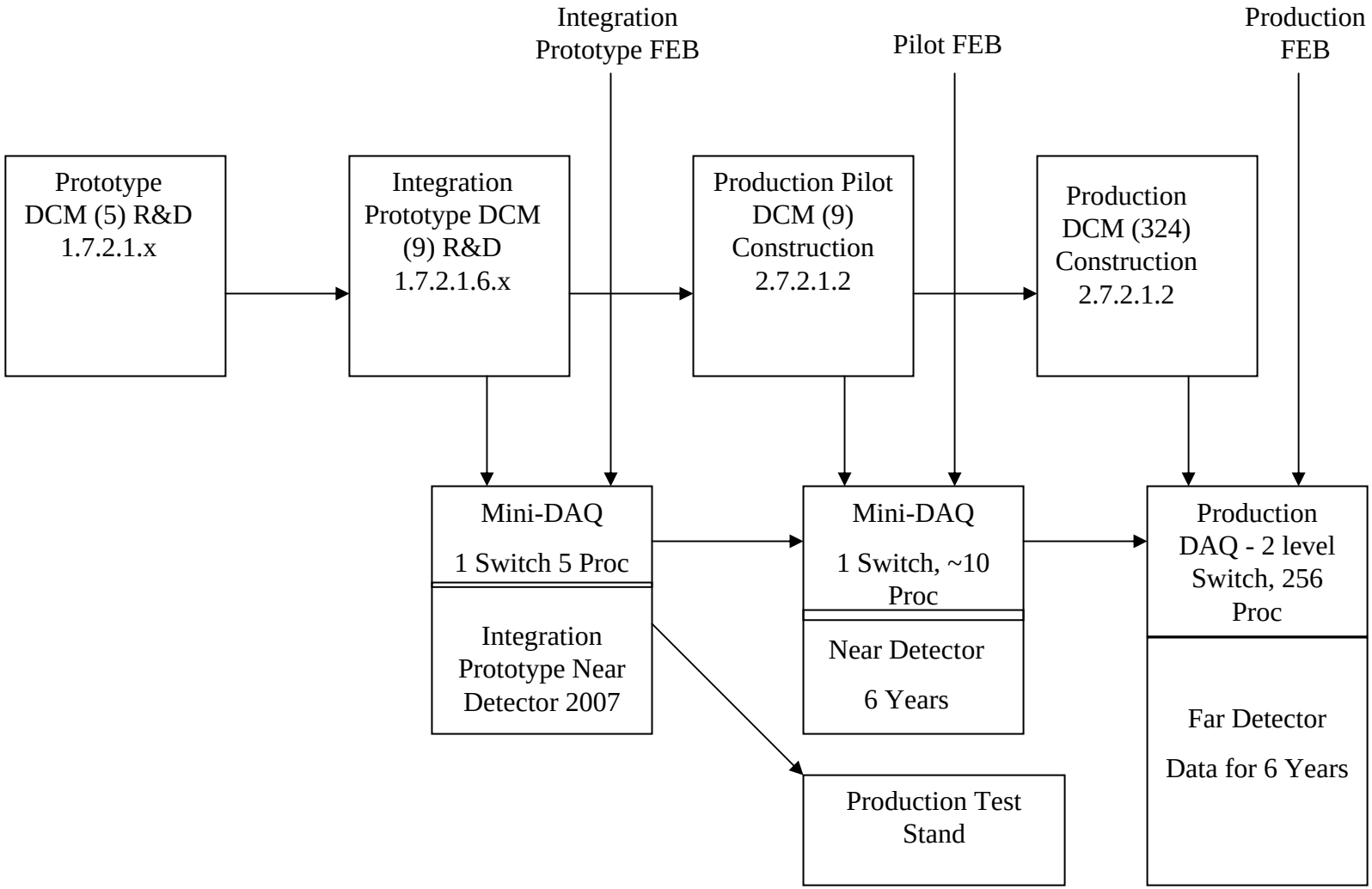
# Dataflow


0a
1a
2a
3a
Switch
Data Concentrators
0b
1b
2b
3b
0c
1c
2c
3c
0d
1d
2d
3d

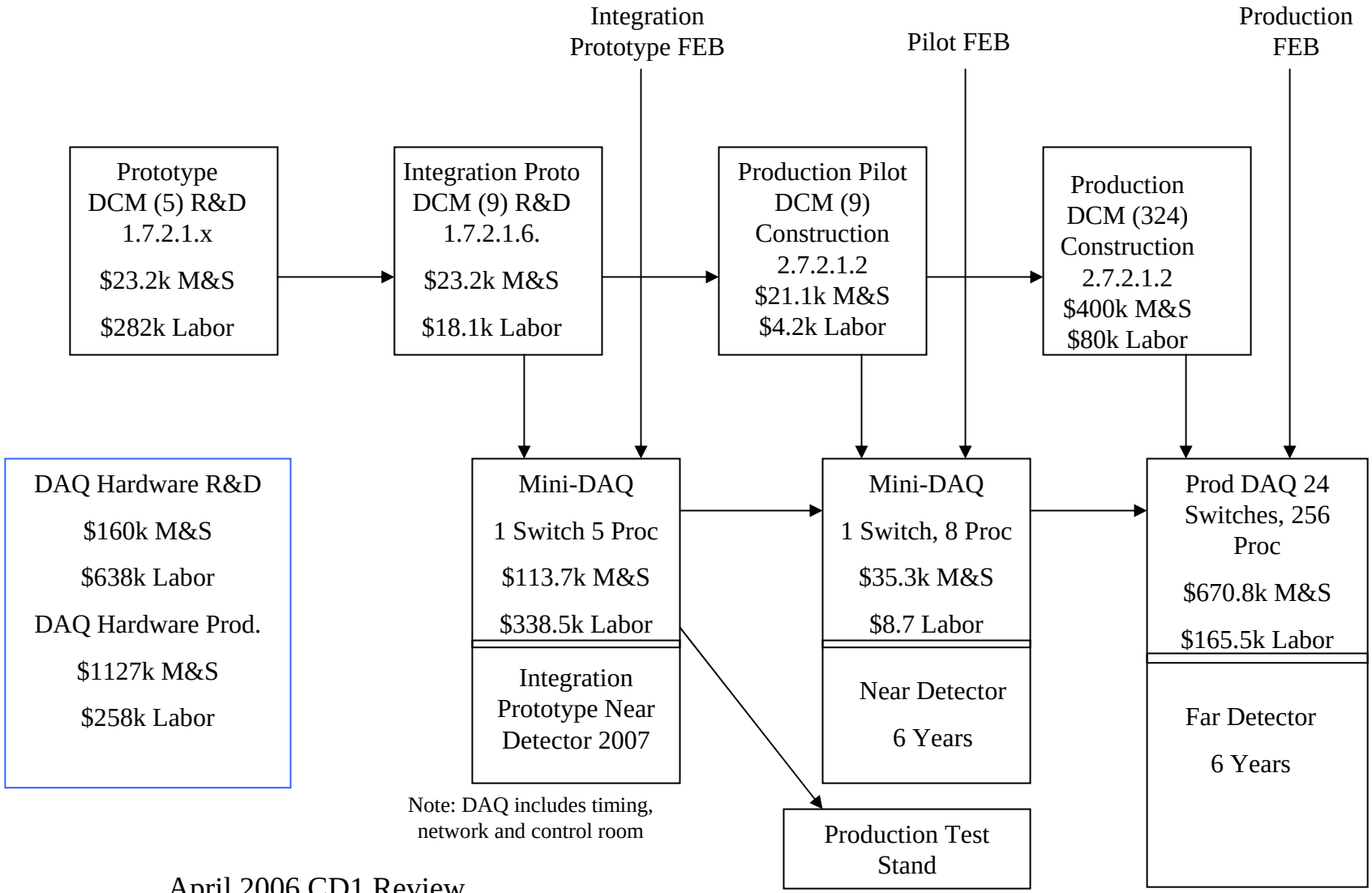
# Dataflow2



# DAQ/DCM Design flow



# DAQ/DCM Cost flow

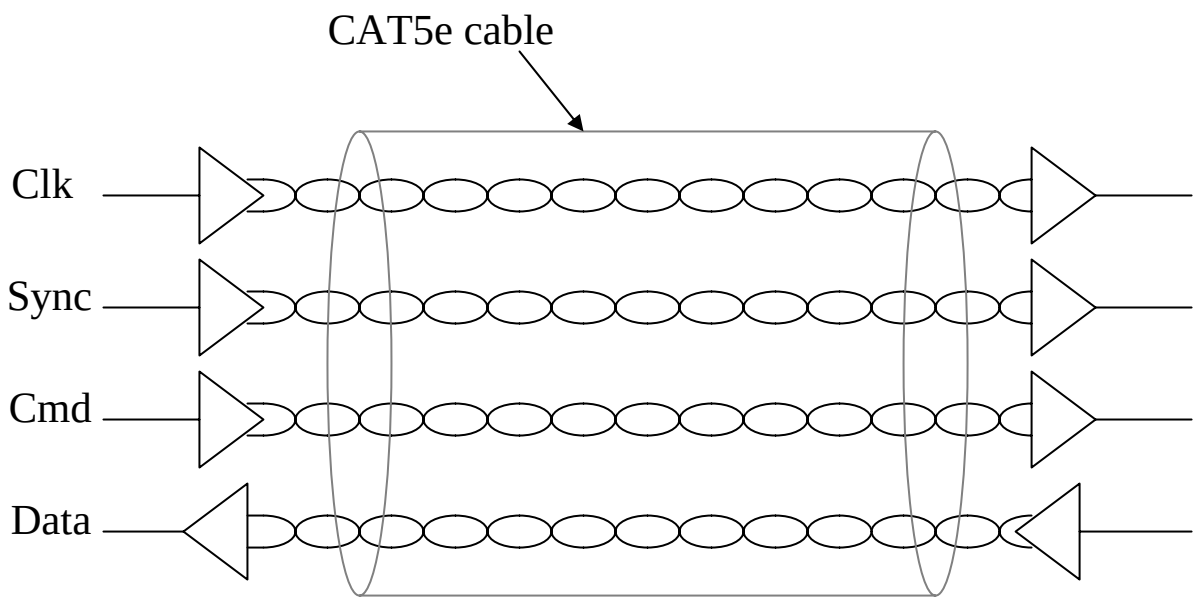



Note: DAQ includes timing, network and control room

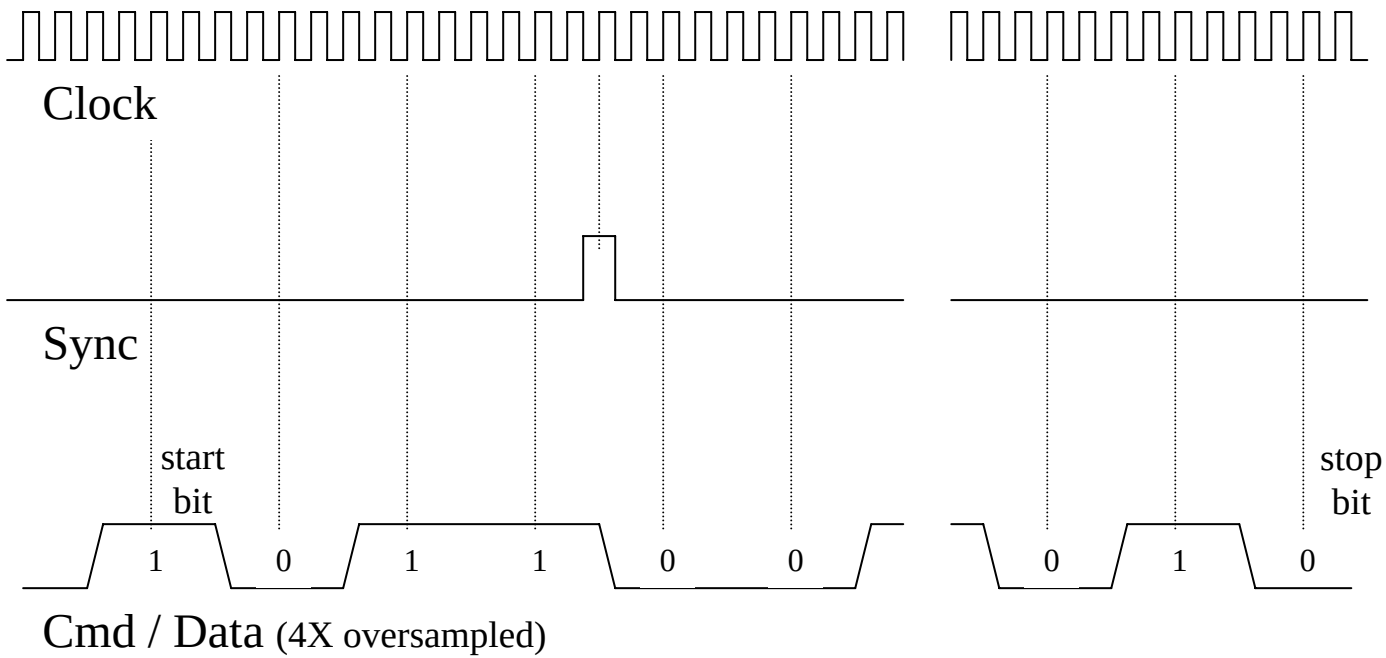
# Finito

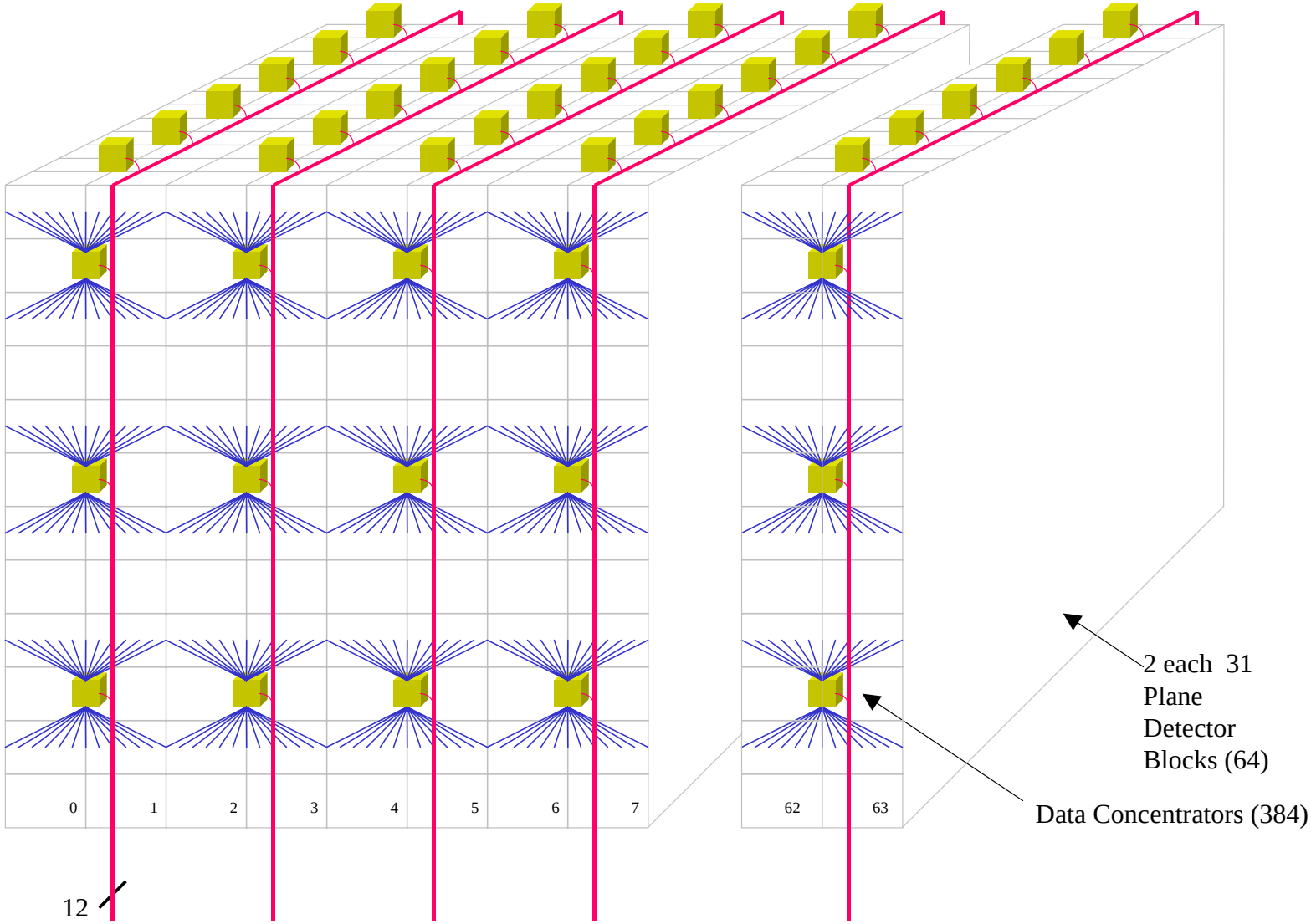
# Backup slides

# DCM Wiring



# DCM Timing


Clock
Sync
start
bit
stop
bit
1
0
1
1
0
0
0
1
0
Cmd / Data (4X oversampled)




Gigabit Ethernet