

Instrumentation Hardware for ILC Accelerator R&D

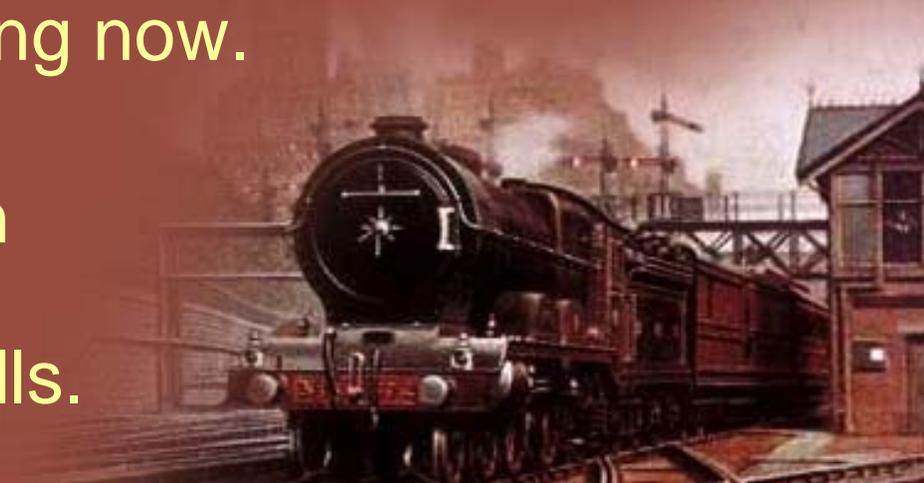


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Electronics Systems Engineering section
of CEPA/CD

Recent History

- 10 years ago the division hardware engineering was more experiment-centric. ESE engineers worked on Fixed Target and Run 2 DAQs and collaborated with PPD on detector R&D.
- We were very involved in the DAQ, Trigger and timing system designs for BTeV and CKM.
- In 2003 we began contributing to the TeV BPM upgrade and that progressed into the MI BPM upgrade which is installing now.
- We quickly learned the signals and timing within the accelerator complex and renewed our RF skills.



SVX-II (SVX 3 IC) Readout System

[Click on Item of Interest](#)

CDF
SVX

SVX-II Silicon Strip Detector System

Number of Channels = 405,504
Level One Trigger Rate = 50 KHz
Level 2 Readout Rate = 1 KHz
Tape Write Rate = 1 to 10 Hz

On-Line Processors Interface System

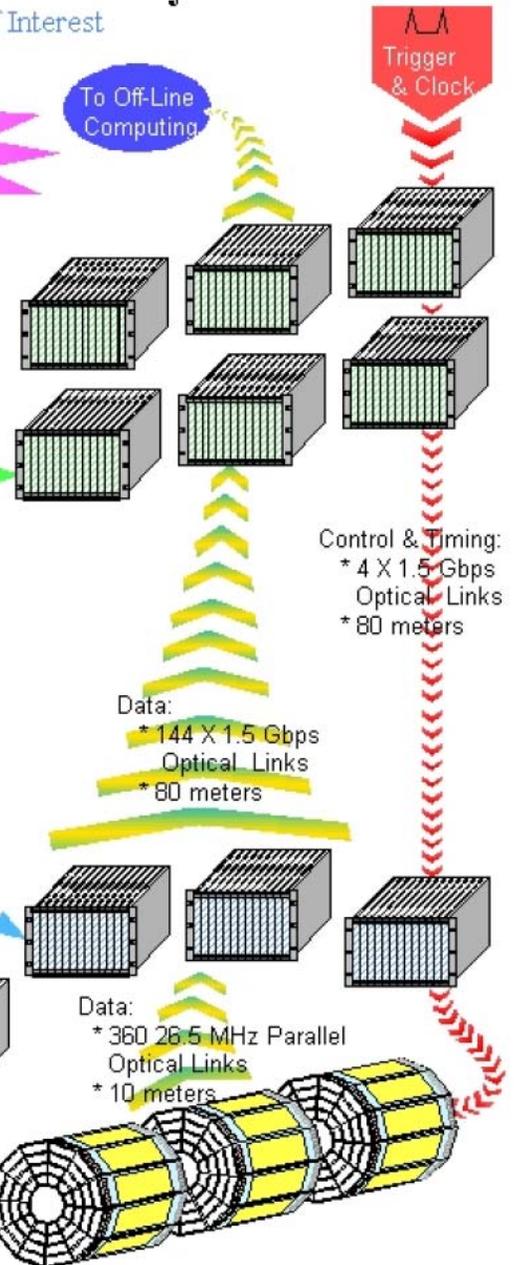
- * 36 - VME Readout Boards (VRB)
- * 36 - VRB Transition Modules (VTM)
- * 1 - VRB Fan Out (VFO)
- * 1 - Silicon Readout Card (SRC)
- * 1 - SRC Transition Module (STM)
- * 1 - VME CPU & 9U Adapter
- * VME Racks, SubRacks & Cables

Detector Area Fast Sequencing Logic

- * 36 - FIB Fiber Interface Board (FIB)
- * 36 - FIB Transition Modules (FTM)
- * 1 - FIB Fan Out Module (FFO)
- * 1 - VME CPU & 9U Adapter
- * VME Racks, SubRacks & Cables

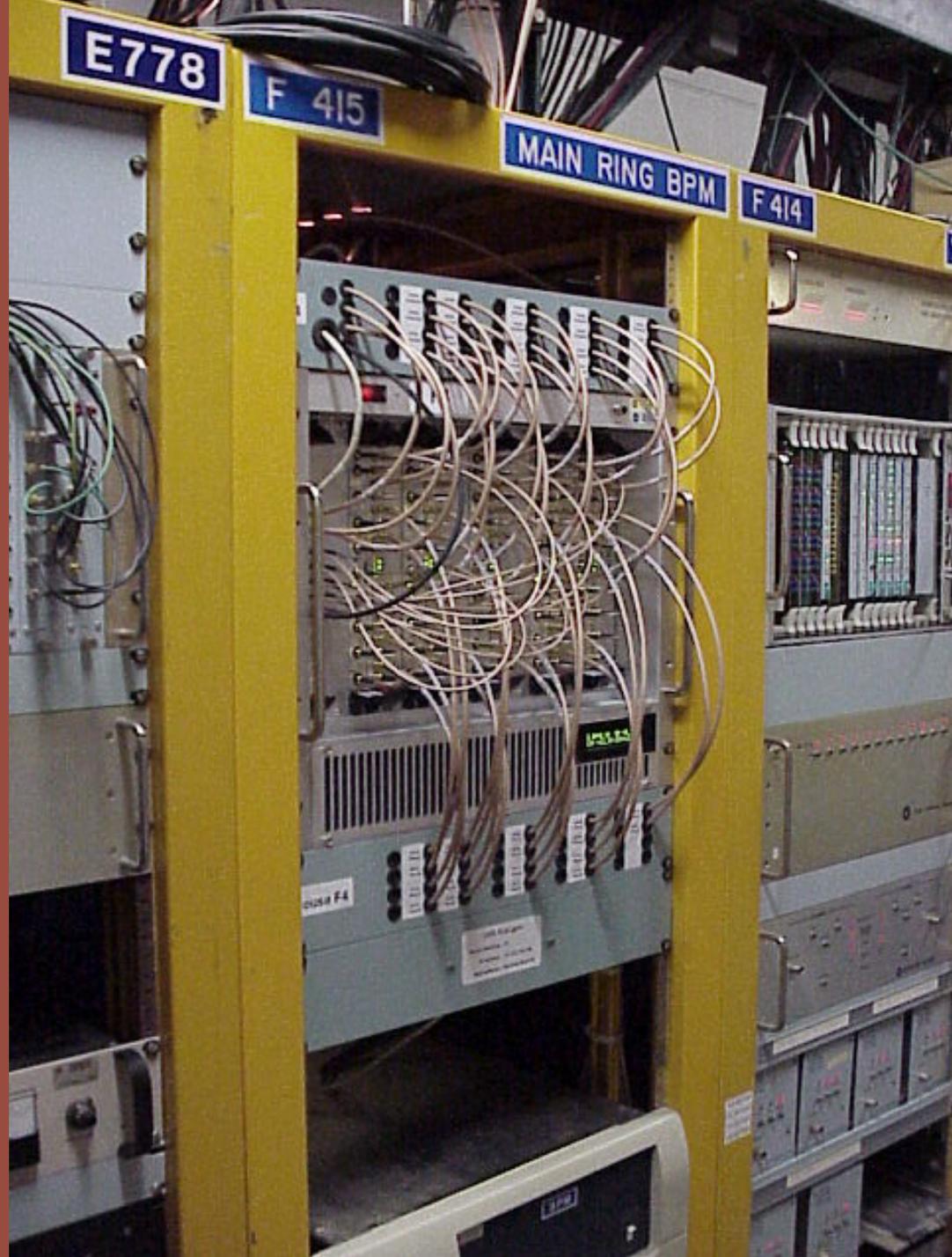
SVX 3 IC Control, Timing & Readout

- * 72 - Port Card (RAD Hard Hybrid)
- * 72 - High Density Interconnects
- * 72 - Flex/Ribbon Junction Box
- * Cables, Connectors

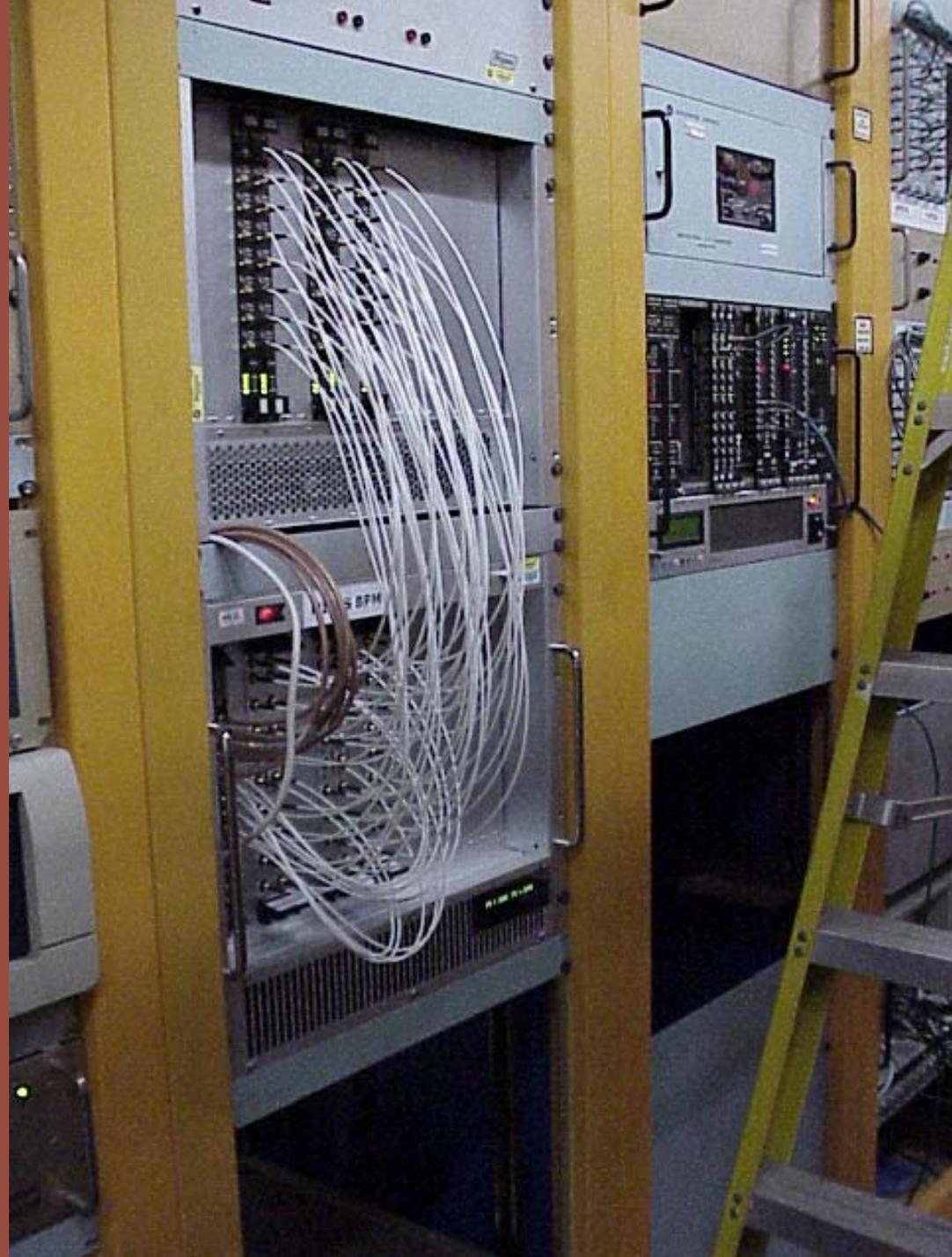


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TeV BPM Installation

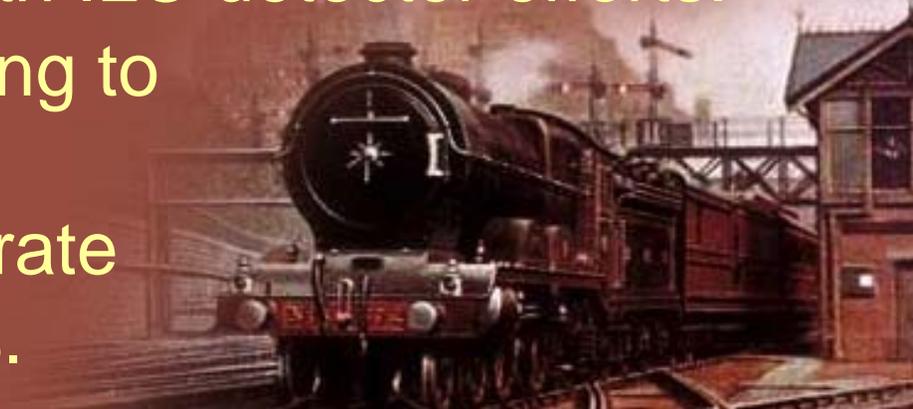


MI BPM Installation



Current ILC

- Hardware support for ILCTA test stand klystron protection systems, 42 modules designed by Peter Prieto, AD. The PCB was designed and the modules built by ESE and ESD.
- Gustavo Cancelo will show the ILCTA cavity control and LLRF activities of our section.
- We are working with ANL collaborators on timing distribution systems and our history of detector R&D is connecting us with ILC detector efforts.
- With SLAC we are working to understand the effect of choosing ATCA as the crate standard for ILC designs.



ILC RDR and WBS

- CD personnel have been involved with the Controls global effort since Snowmass last year when it was Global Group 2.
- I am supporting the Controls area costing effort lead by John Cowardine, ANL, by providing standard packaging costing and guidelines, costing for specific hardware as requested and collaborating on the overall system architecture.



Down the Track

- We are a proven collaborator that plans to contribute hardware engineering to controls, instrumentation, detector and test beam tasks.
- We have a disciplined approach to engineering that produces robust designs which meet the customer requirements.
- We understand hardware standards and utilize them where appropriate for cost efficiency.



Finito

