

Project Status

Electronic Systems Engineering

Vince Pavlicek

April 10, 2007



Outline

- **Groups and projects**
 - DAQ, Control and Timing, Detector Instrumentation, & Engineering Support
- **Effort allocation last quarter**
- **Updates on current project status**
 - SNAP
 - Phenix
 - NOvA
 - ILC LLRF
 - ILC detector R&D
 - CDF and D0 Run 2
 - Accelerator – IPM, MI BPM, TeV BPM
- **Future projects**
 - CMS R&D for SLHC
 - ILC test beam at MTest
 - MICE





DAQ, Control and Timing Group

Bill Haynes, GL

Tom Boes

Gustavo Cancelo

Greg Deuerling

Rick Kwarciany

Neal Wilcer

Project portfolio

- ILC LLRF and Cavity Control
- NOvA DAQ hardware
 - Data Combiner Module prototype
 - Timing distribution system
- Equipment support

Core competencies

- Control systems
- Firmware
- DAQ systems
- VME & PCI
- CDF & D0
- Timing algorithms





Detector Instrumentation Group

Alan Prosser, GL

Jeff Andresen

Stew Bledsoe

John Chramowicz

Hank Connor

Ryan Rivera

Marcos Turqueti

Project portfolio

- Phenix
- CMS
- SNAP
- ILC detector R&D
- Equipment support

Core competencies

- Multichip modules
- Test stands
- Front end design
- ASIC specs
- Wire bonding
- Thick and thin film
- Firmware





Engineering Support Group

Vince Pavlicek, GL

Bill Barker

Jim Franzen

Rick Mahlum

Thinh Pham

Ken Treptow

Ted Zmuda

Project portfolio

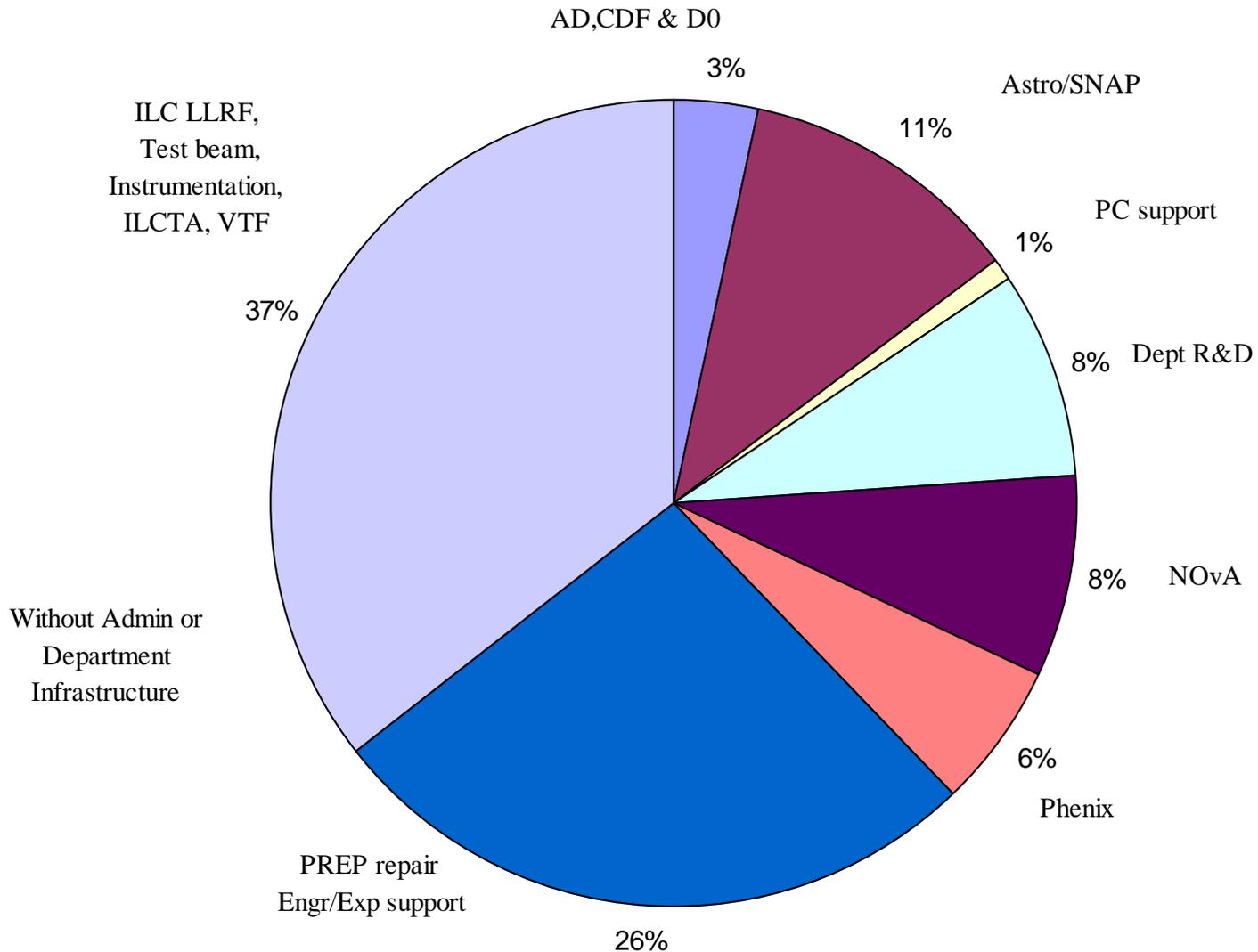
- ILC costing and HA hardware
- Run 2
- ILC LLRF support
- Interface to CD logistics
- PREP support
- NOvA support

Core competencies

- CDF & D0 hardware
- Project management
- PCB layout
- PREP customer support
- Equipment repair

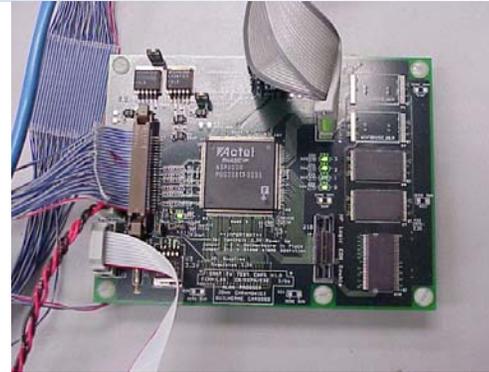


Effort Report for Feb+Mar '07



Project Status - SNAP

- **Data Compression**
 - CCSDS Lossless
 - Square root prescaler
 - Both techniques implemented in firmware
- **Slice Command and Response**
 - ICU Control Interface implemented in firmware
- **Downlink Controller**
 - Multislice Architecture being defined
- **FRICO ASIC Testing**
 - Chip tested at 140 deg K
 - Functionality and stability tested
- **IEEE RealTime 2007 Paper (A. Prosser et. al.)**
- **ESE Effort:**
 - 2.0 - 2.5 FTE
- **Stakeholders:**
 - John Chramowicz, Hank Connor, Greg Deuerling, Alan Prosser, Ryan Rivera, Marcos Turqueti



Slice Card Development



Flash Memory Testing

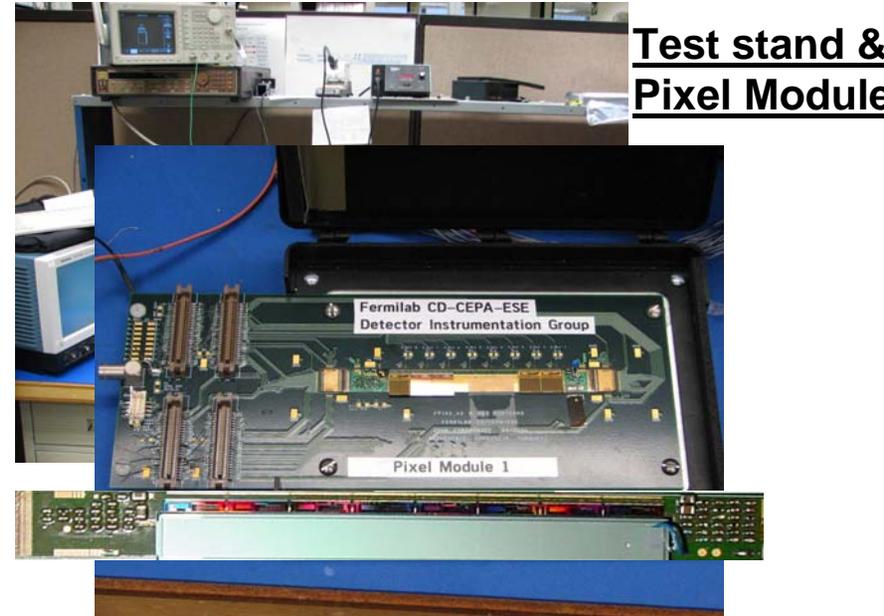


ASIC Test

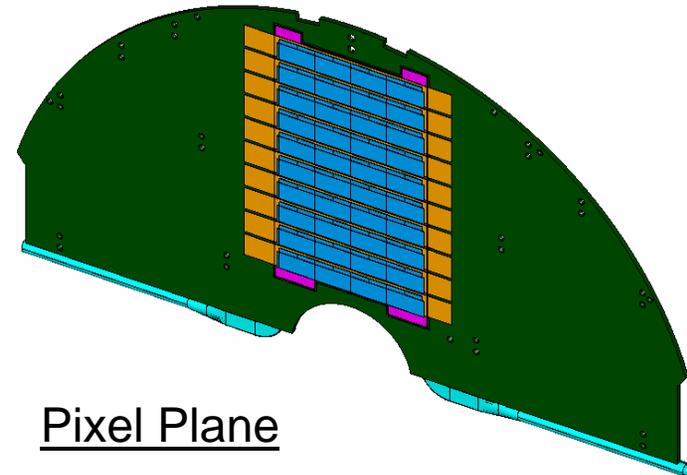


Project Status - PHENIX

- **Pixel Module Test Stand**
 - Development complete. In use by multiple parties.
- **KISS High Density Interconnect**
 - Simplified HDI designed and tested.
- **FPIX 2.1 Wafer Probe Automation**
 - Software developed for PPD to automate wafer testing.
- **Pixel Plane PCB**
 - PCB is in fabrication
 - Preparing for arrival of PCBs (assembly and test).
- **ESE Effort:**
 - 1- 2 FTE
- **IEEE RealTime 2007 Paper (R. Rivera, M. Turqueti)**
- **Stakeholders:**
 - Jeff Andresen, Stew Bledsoe, Hank Connor, Ryan Rivera, Marcos Turqueti



Test stand & Pixel Module



Pixel Plane



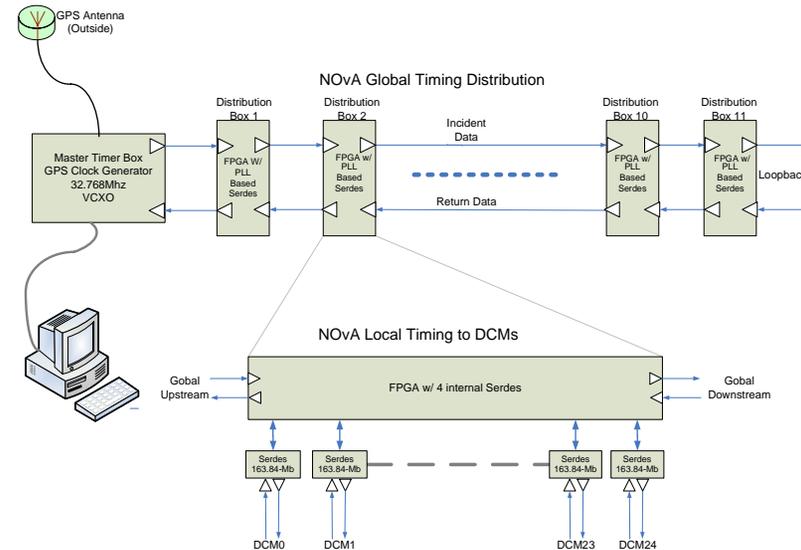
Project Status - NOvA

- **Data Combiner Module Prototype:** Two Assembled boards having firmware and software tested. This design contains more than the required functionality and could be used for the Near Detector test Dec 2007. Picture follows.

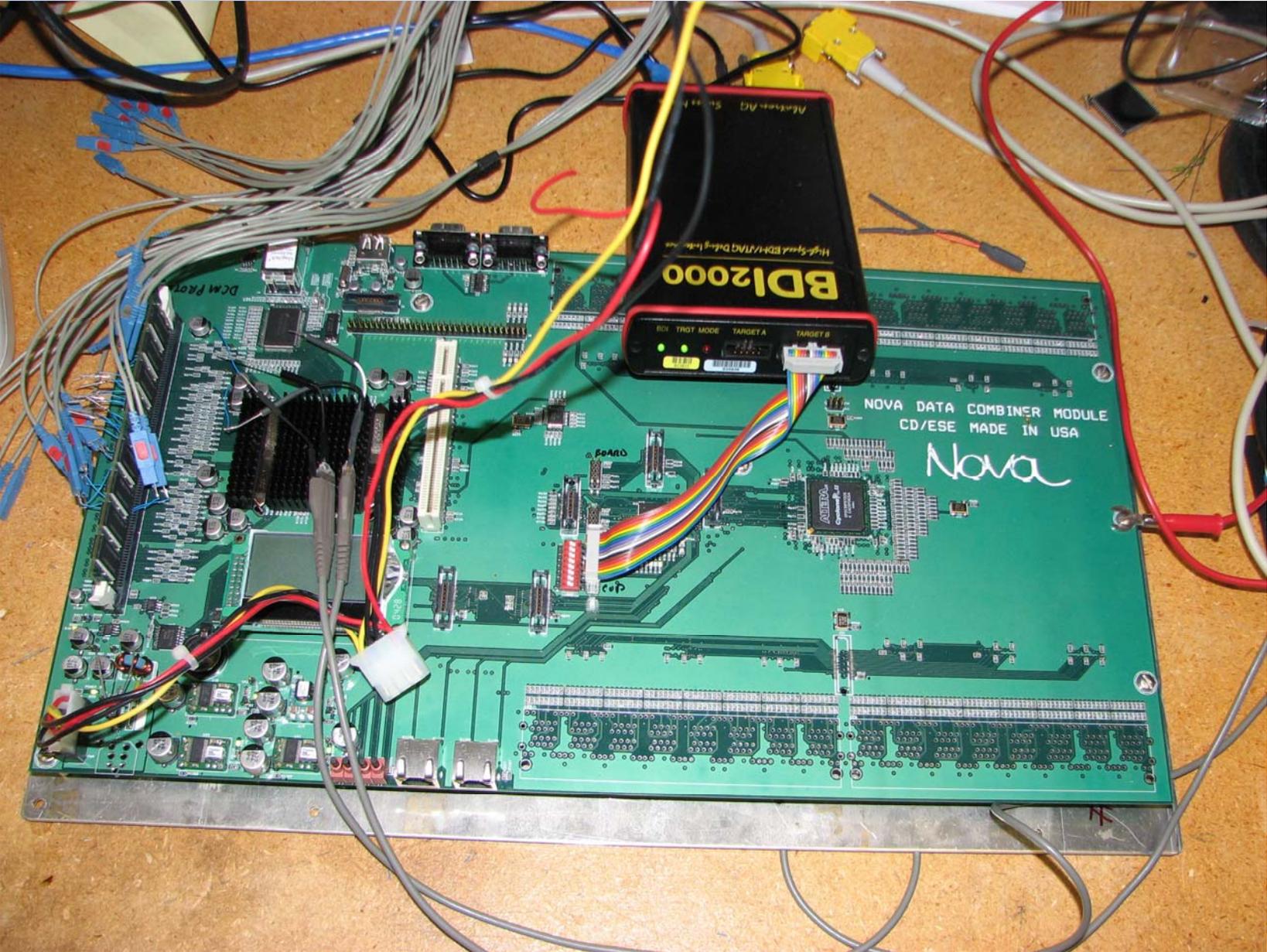
- **Timing system:** System architecture has been proposed, accepted and being integrated with the far detector cooling and power distribution design going on now. Schematic for prototype distribution card underway.

- **ESE Effort:** 1.5 FTE from Bill Haynes, Rick Kwarciany, Jim Franzen & Vince

- **Directors review June 4-6, CD2/3a review July 17-19**



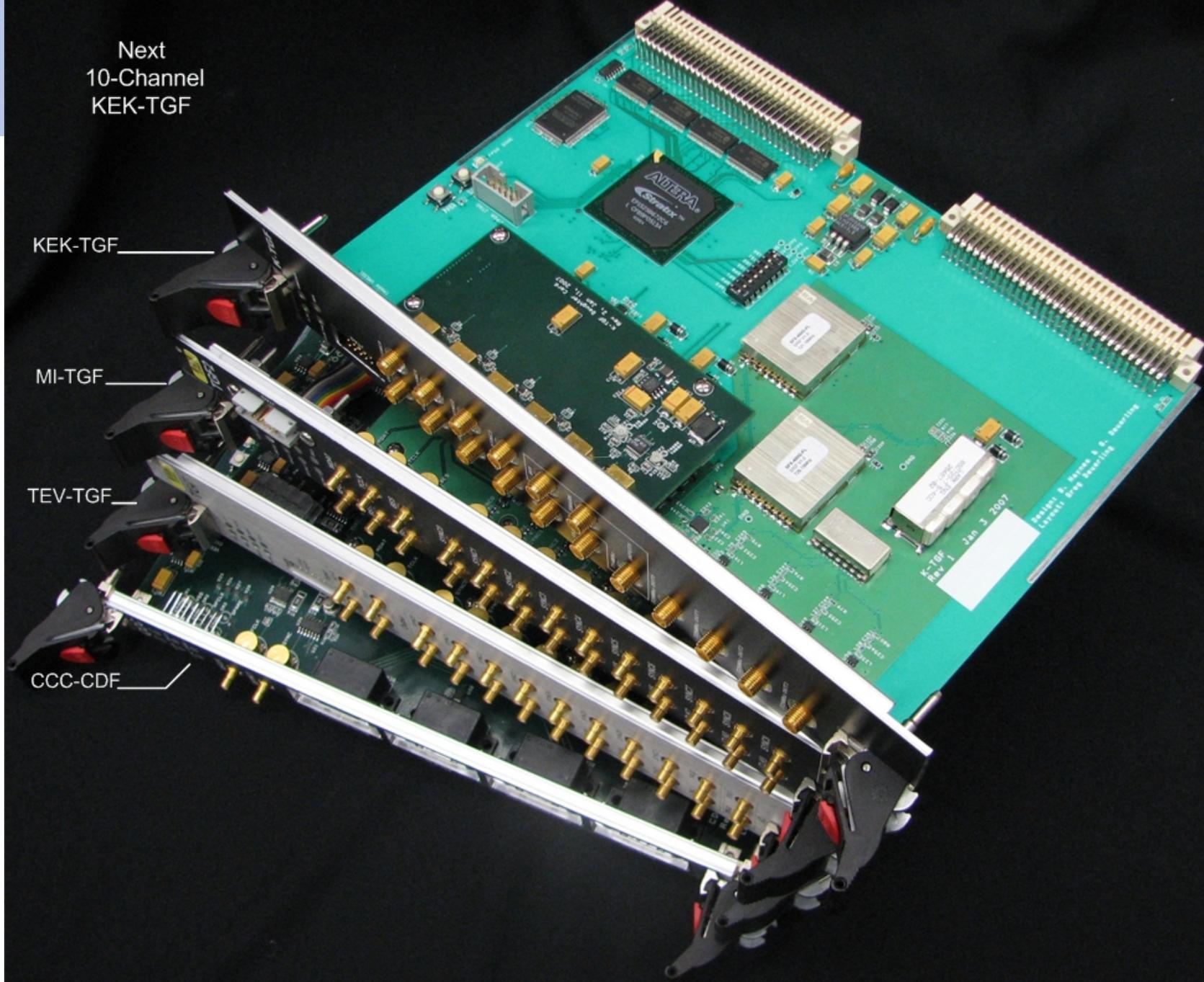
DCM Prototype





Next
10-Channel
KEK-TGF

We
Recycle



KEK-TGF

MI-TGF

TEV-TGF

CCC-CDF

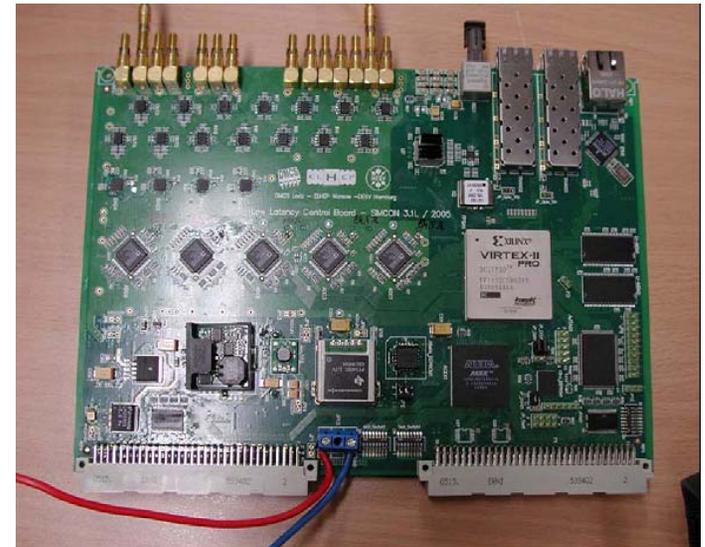


Electronic Systems Engineering

Project Status - ILCTA & LLRF

- **FNAL LLRF controller update:**
Partially assembled digital sections mostly tested. Analog sections now being assembled. Pix follows
- **DESY Simcon Low Level RF Controller:** new Intermediate Frequency processing reported on already. Still supporting CC2 testing at Meson lab
- **Gustavo Cancelo, Ted Zmuda, Rick Kwarcianny, Ken Treptow, and Neal Wilcer**

DESY's SIMCON



SRAM (one chip on bottom side)

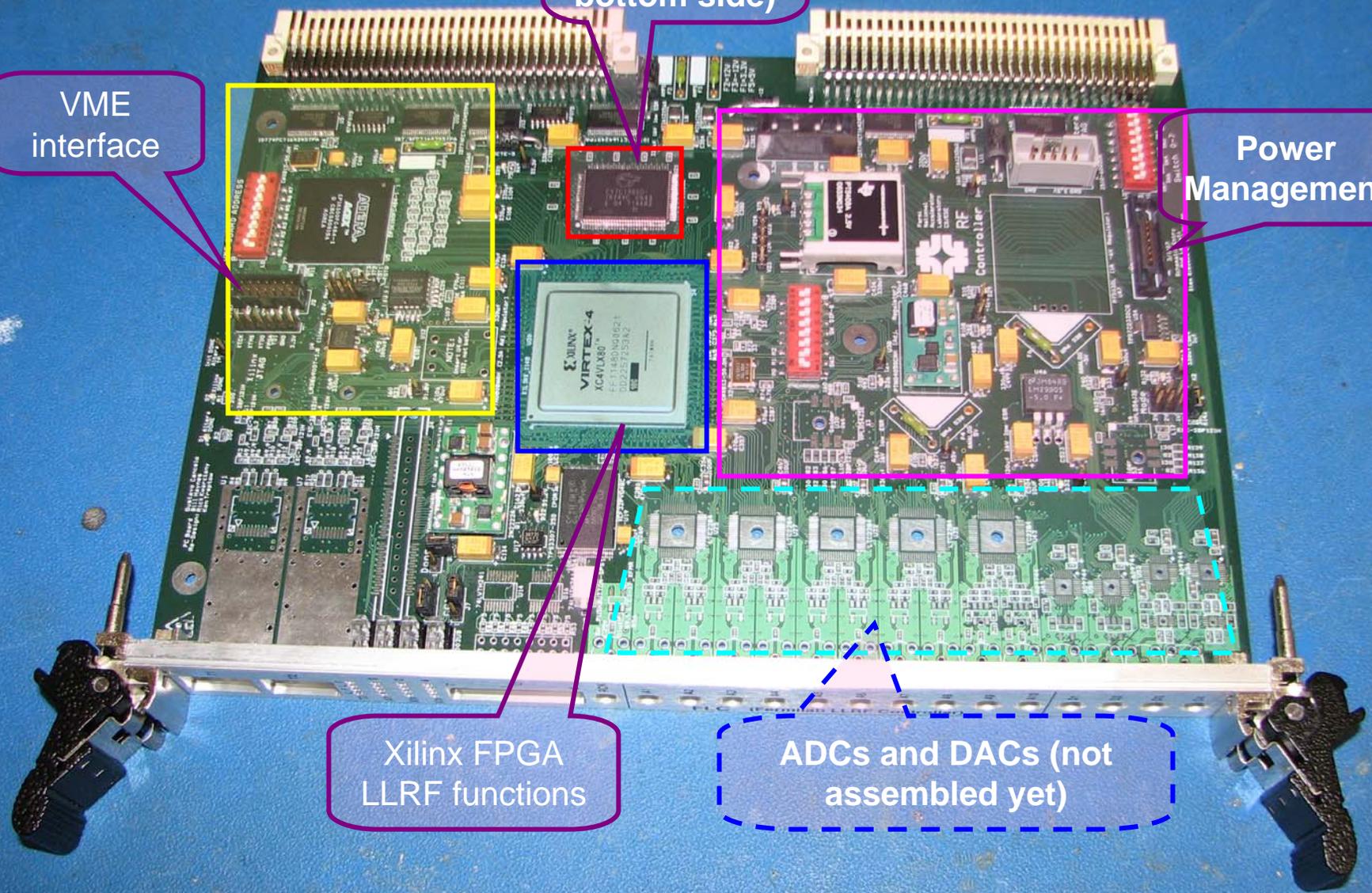
VME interface

Power Management

Xilinx Virtex-4
XC4VX80
FF11480NG0C24
002257259AZ

Xilinx FPGA
LLRF functions

ADCs and DACs (not assembled yet)





Project Status - Support

Accelerator and Running Experiment systems

- **MI BPM, TeV BPM, TeV IPM - Haynes, Treptow, Kwarcianny**
 - Occasional consultation and, more rarely, support.

- **CDF and DO – Haynes, Chramowicz, Pham, Treptow, Pavlicek, Zmuda.**
 - Test stand repairs, occasional diagnosis of odd card behavior.
 - CAEN High Voltage support including adapter cables for new supplies.

- **SciBooNE – Mahlum, Connor, Bledsoe**
 - Signal issues with a discriminator.
 - High Voltage issues.

- **Misc**
 - Two Labview & CAMAC based test stands, MiniBooNE and ILC.





Future Projects – CMS Upgrade

- **ESE Participation in ACES Workshop (CERN)**
- **Having Discussions with Fermilab scientists on collaborating**
 - **Leverage BTeV and CMS forward pixels experience**
- **Participation in Upcoming Visit by Jordan Nash (Imperial College, UK)**
 - **Stacked Tracking, Pixel Detector for L1-Triggering**





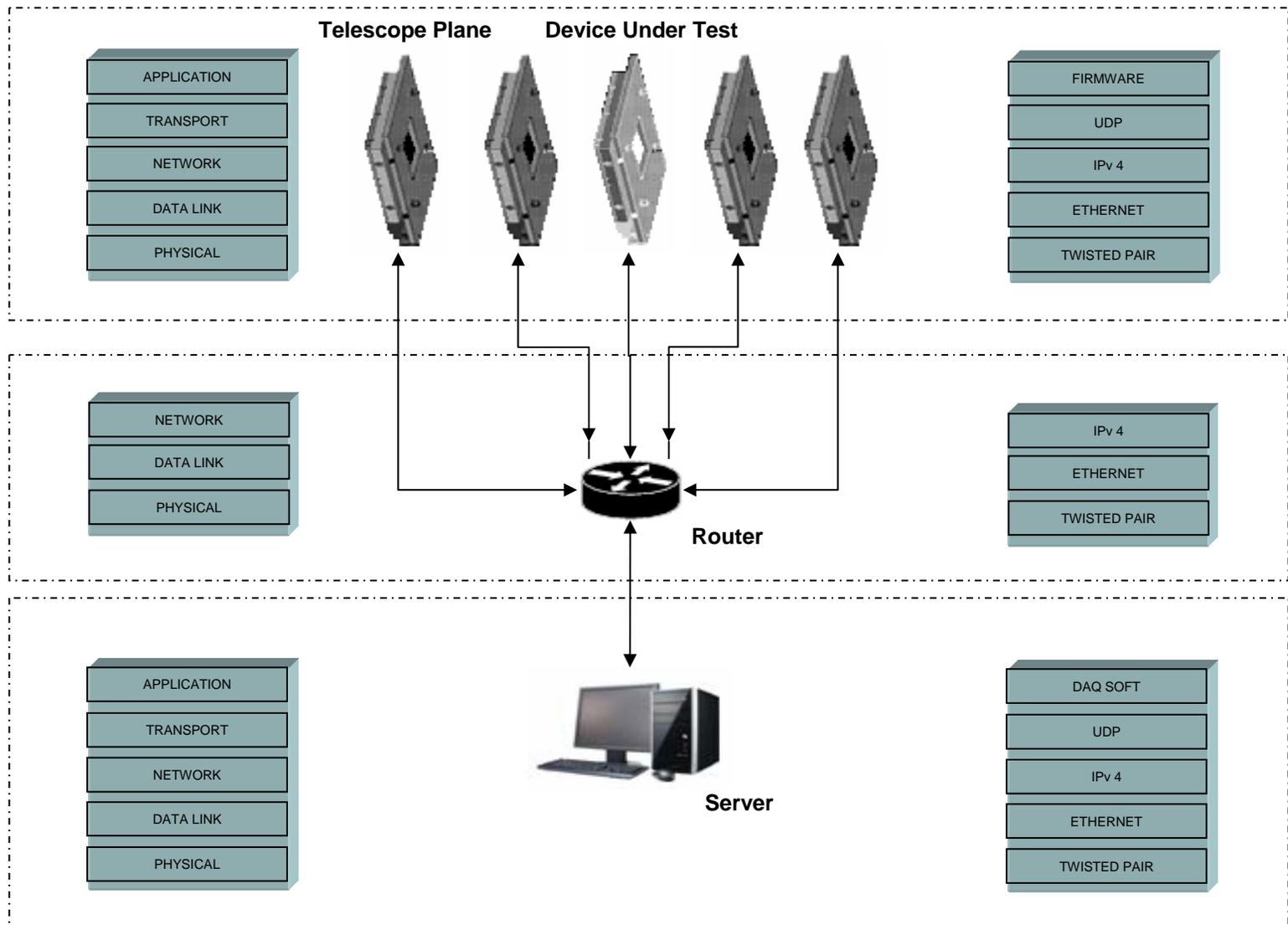
Future Projects – ILC Detector R&D

- **Test beam facility at M-Test**
 - Integrated Telescope Architecture has been proposed (R. Rivera, M. Turqueti)
 - Implementation: Approval Pending(?)
 - IEEE RealTime 2007 Paper (M. Turqueti et. al.)

- **Participating in Weekly Pixel R&D meetings**
 - Investigating Serial Powering Techniques for Pixel Chips



Integrated Telescope Architecture





CDF Projects on hold

- **CEAN Power Supply Radiation Tolerance**
 - CAEN High Voltage power supplies are in the collision hall and demonstrate problems indicative of single event upset (SET).
 - Investigate specifics of problems and software changes.
 - Vince Pavlicek, Rick Tesarek (CDF), Silicon SPL.
- **DOIM Receiver - Bit Booster**
 - Radiation damage is reducing the light output of the fiber optic link transmitters. They can be turned up but that happens in groups of 9*5 and in 4 or 5 groups the brightest bit is too bright for the receiver. We are investigating making a new wide range receiver.
 - Small prototype built with support from CDF. Need design resources. Current prototype works. Need production layout.
 - Ken Treptow, Silicon SPL
- **Low priority now that the beam losses have been reduced.**
May become more important as the luminosity grows.

