PHENIX Pixel Plane Project Closeout Report

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Summary:

The Electronic Systems Engineering department of the Computing Division (CD/ESE) at Fermilab participated in a work program for PHENIX project. This program was governed by a Statement of Work entered into with the Los Alamos National Laboratory (LANL). The project was assigned Fermilab Task Code R3L106. As of Sept. 1, 2007, all of these tasks have been completed. This document provides a description of the work carried out and the items delivered. It includes a list of relevant documentation.

Statement of Work:

There are two relevant documents that define the work to be undertaken by ESE. These documents are:

1. Statement of Work (SOW) by Computing Division at Fermilab for PHENIX Silicon Pixel Detector Project at Los Alamos National Laboratory During Fiscal Year 2006, Issue Date March 2, 2006, Revision 1.0. This document may be found in the Computing Division Database (document number CD-doc-2391-v1).
2. Subcontract Award/Purchase Order Modification for Contract 38480-001-06 C2 (modification 1). This document may be found in the Computing Division Database (document number CD-doc-2391-v1).

These two documents specify that Fermilab would provide designs for:

1. A Pixel Module Test Card. This card is also referred to as a Port Card. This provides the means to test a pixel module which has been wire bonded to a flexible circuit High Density Interconnect (HDI).
2. A Pixel Plane Printed Circuit Board (PCB). This design is to support up to 10 pixel detector modules and HDIs with 8 pixel chips each.

3. A Test Stand for testing the pixel detector modules. This includes the firmware and software to interface to a port card and execute tests.

Figure 1 shows a picture of the Port Card with a KISS HDI and Hybrid attached for testing:

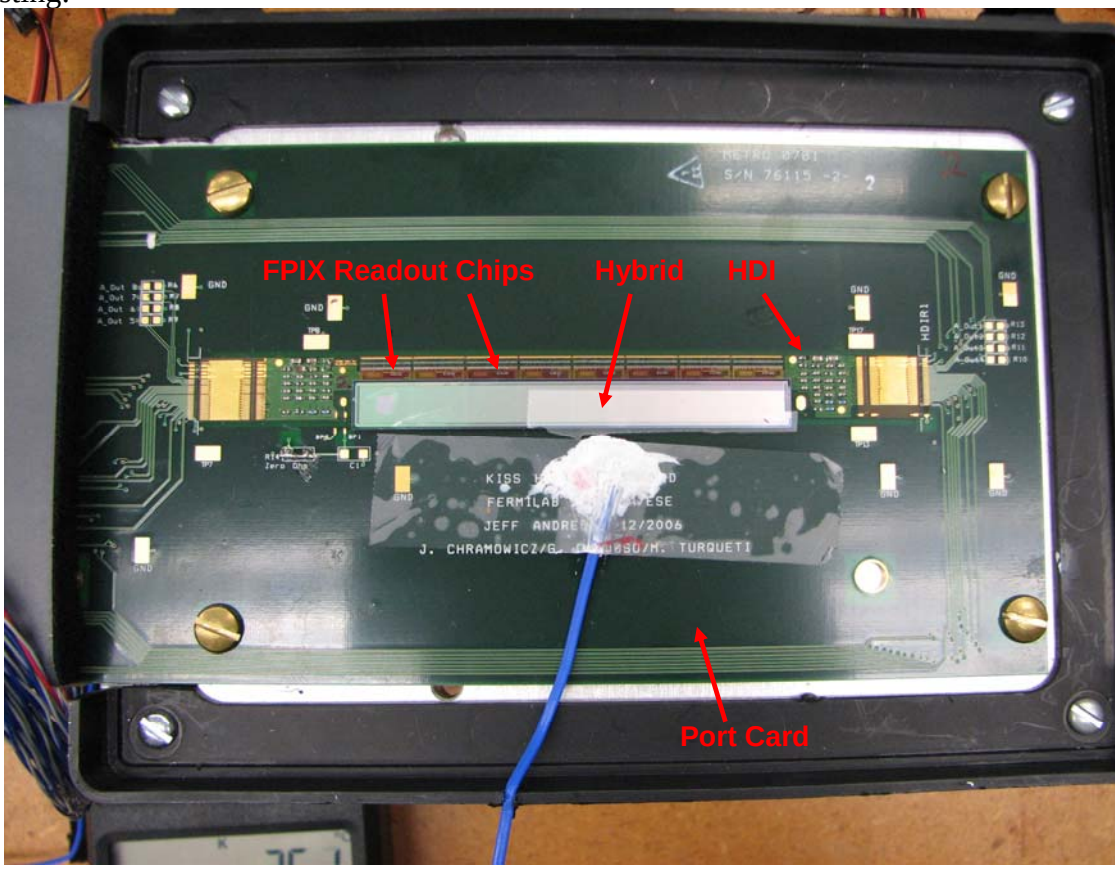


Figure 1:
Port Card with KISS HDI and Hybrid

Figure 2 shows a picture of the Pixel Plane PCB with KISS HDI /Hybrids attached:

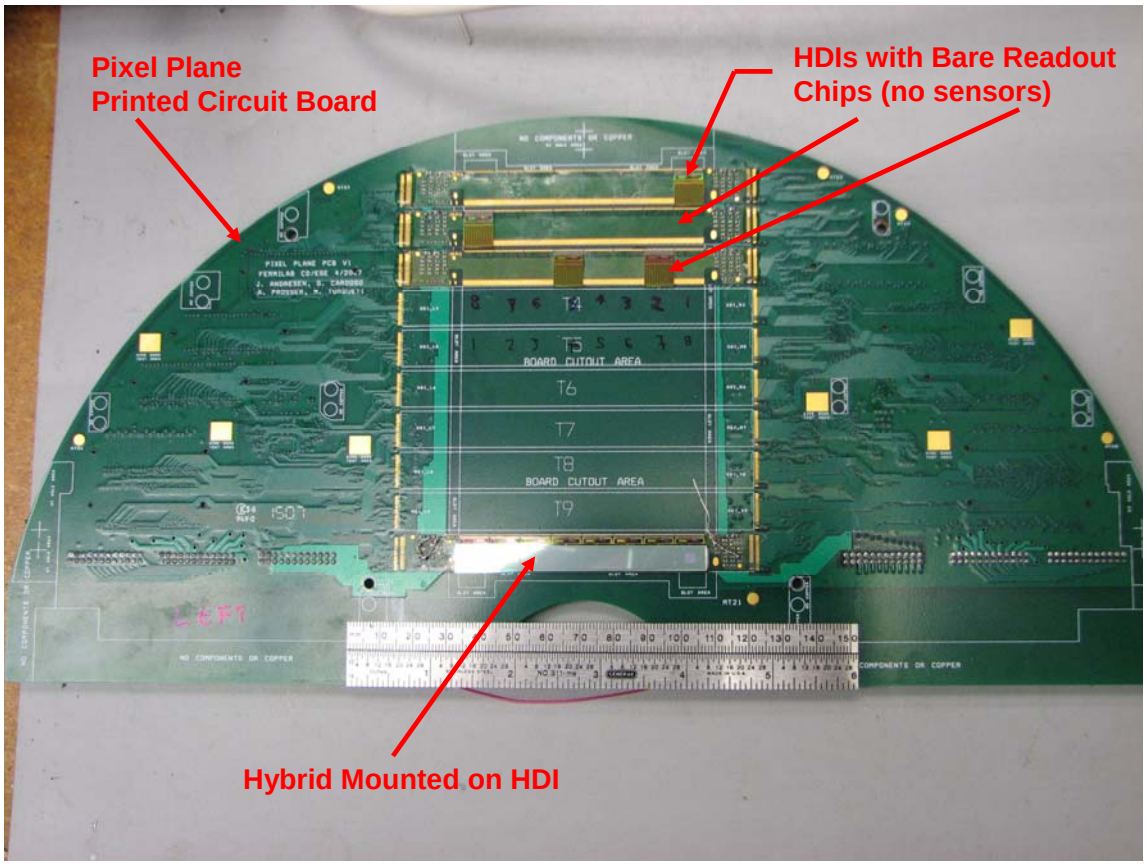


Figure 2:
Pixel Plane PCB with KISS HDI/Hybrids

Figure 3 illustrates a complete test stand with a port card for test and running the Pinga test stand software.

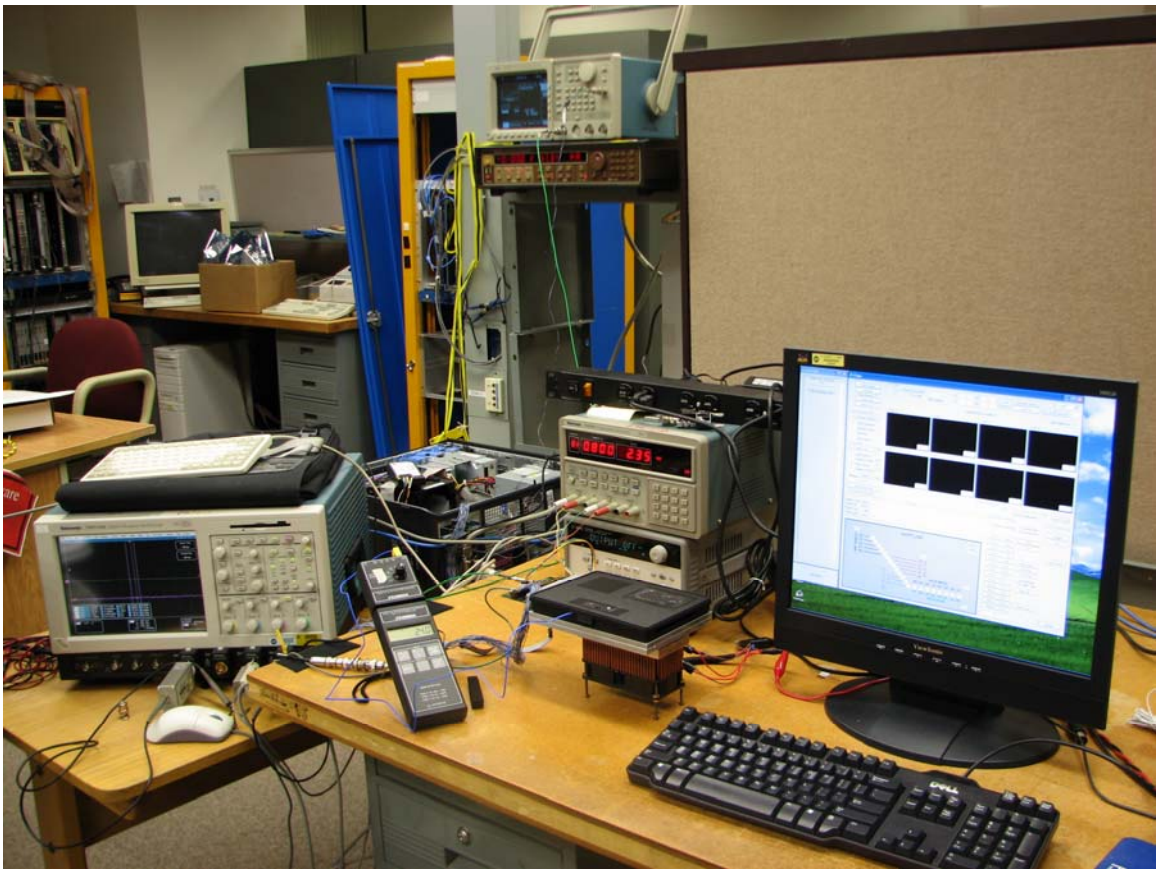


Figure 3:
PHENIX Hybrid Test Stand

Figures 4 and 5 illustrate the graphical user interface and some of the analysis features that are available with the Pinga test stand software:

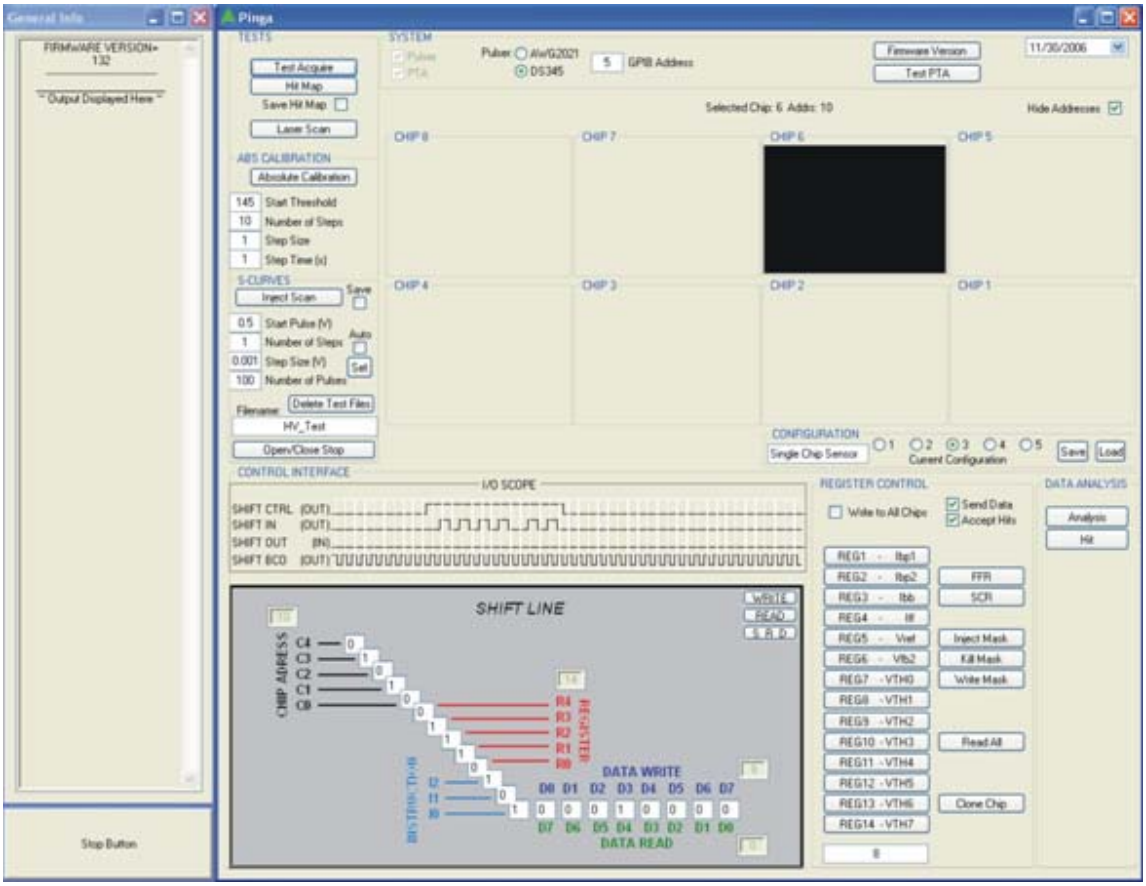


Figure 4:
Pinga GUI

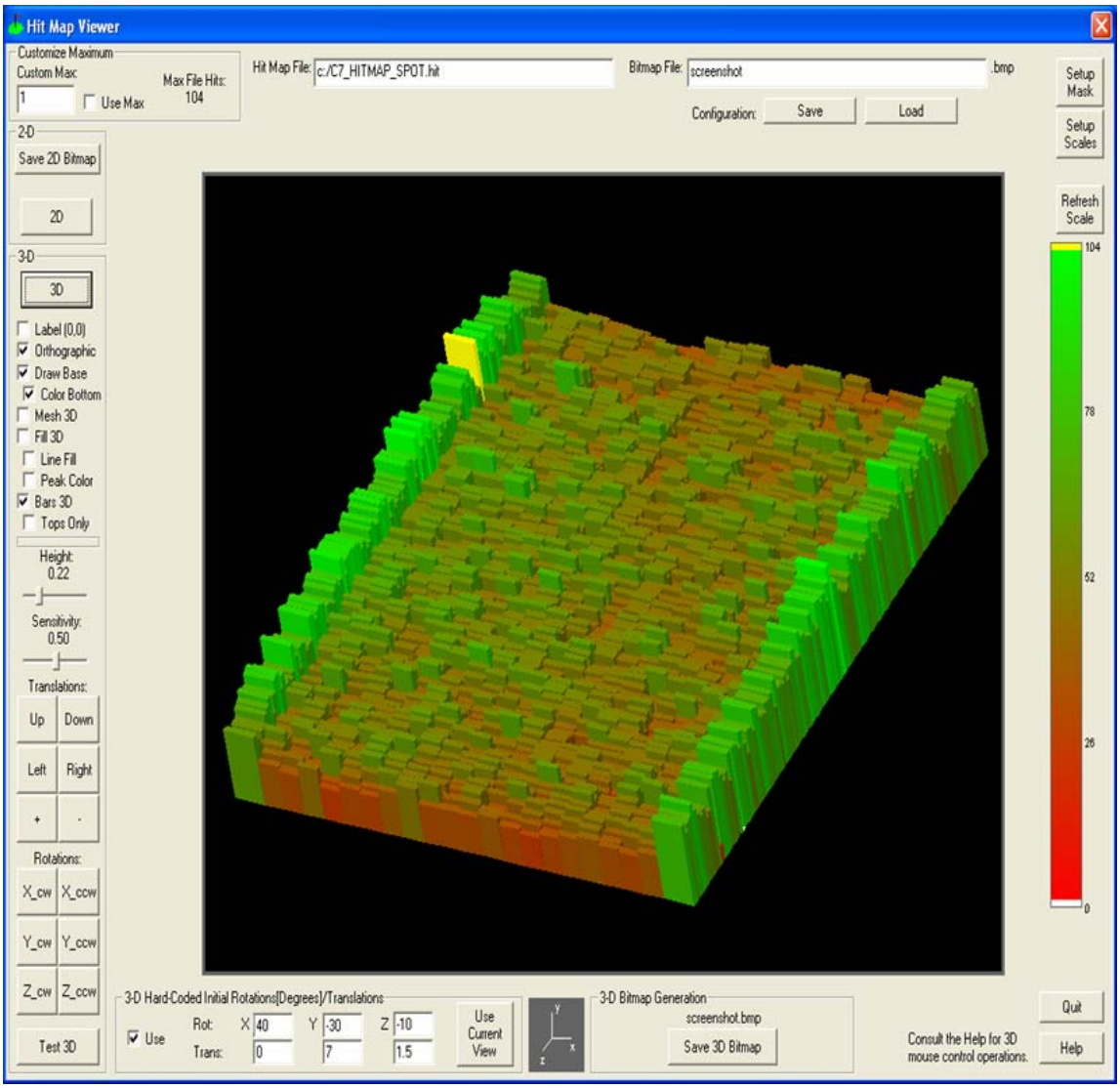


Figure 5:
Pinga Hit Map Viewer

In addition to these products, there were significant contributions made on behalf of the project by ESE engineers for activities that were not covered in the statement of work or the subsequent modification. A wafer probe test station was automated for the Electrical Engineering Department of the Particle Physics Division (PPD) on the 14th floor of Wilson Hall. This station made automated testing of the FPIX2.1 pixel detector readout chip wafers possible in a much smaller time period than was previously required. In addition to the time to develop the automated solution, support and training for this probe station was provided. The design activities of the HDIs themselves were also not covered in the statement of work or the modification.

During the course of the project, there were difficulties encountered due to leakage current induced instabilities in the FPIX2.1 pixel readout chip. Detailed investigations of

the nature of the instabilities and insight into feasible solutions were made possible through the use of a PCI Test Adapter, version 2 (PTA2) based test stand that was provided to the ASIC design group of PPD. This support also fell outside of the boundaries outlined in the statement of work.

ESE Participation:

Members of the ESE department who participated in this work included the following:

Jeff Andresen was the layout engineer for the KISS HDIs, the version 1 Port Card, and the Pixel Plane PCB. He also worked closely with mechanical engineers from HyTech and Particle Physics Division of Fermilab on mechanical design issues. He was also responsible for working with vendors to have HDIs and PCBs fabricated.

Stew Bledsoe provided parts procurement and board assembly services.

Guilherme Cardoso provided design expertise and Technical Project Management support.

John Chramowicz was the layout engineer for the version 2 Port Card and provided board assembly and wire bonding services.

Hank Connor provided wire bonding services.

Greg Deuerling provided support for the PTA2 which forms the foundation of the test stand hardware.

Ryan Rivera developed test stand software for the project. He also worked closely with members of PPD and LANL to train them in the use of the software and the test bench hardware. Ryan also participated in much of the testing undertaken by ESE.

Marcos Turqueti was the electronics designer of the Pixel Plane PCB. He also performed much of the testing undertaken by ESE. Marcos also provided training expertise.

The following chart illustrates the effort reported against the ENGINEERING SUPPORT/PHENIX Silicon Pixel Detector Project - LANL budget code for all ESE personnel during the duration of the project:

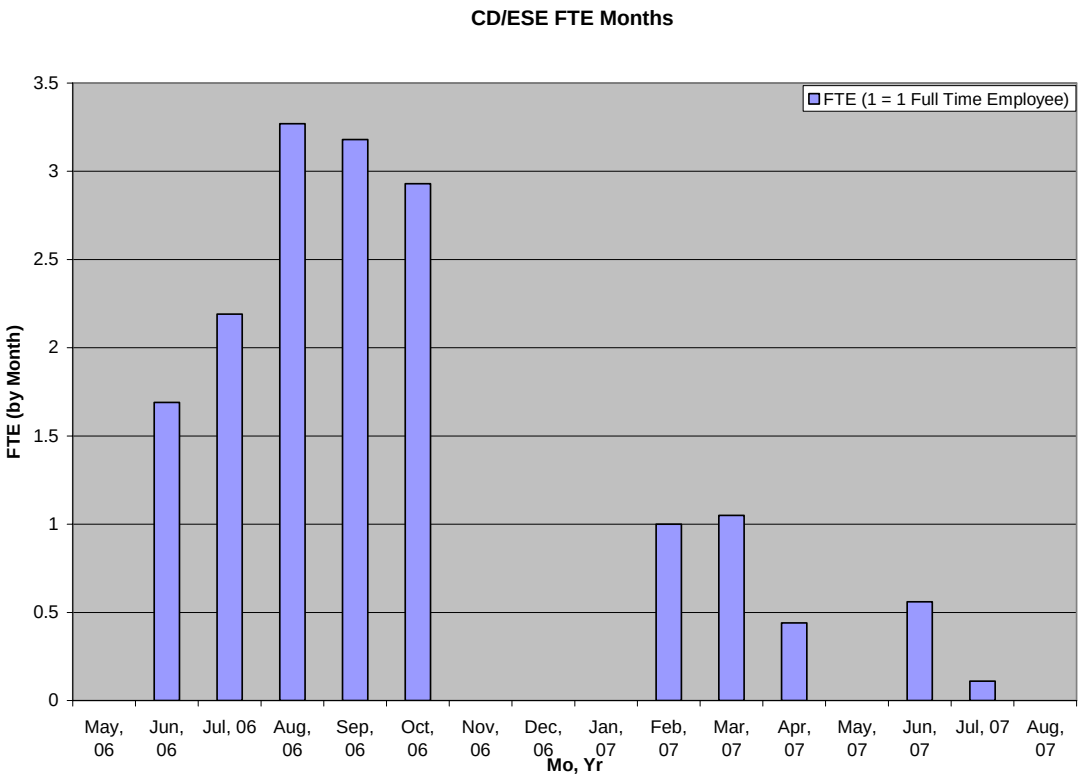


Figure 1
CD/ESE Effort by Month

The following chart illustrates the expenditures for the project by month:

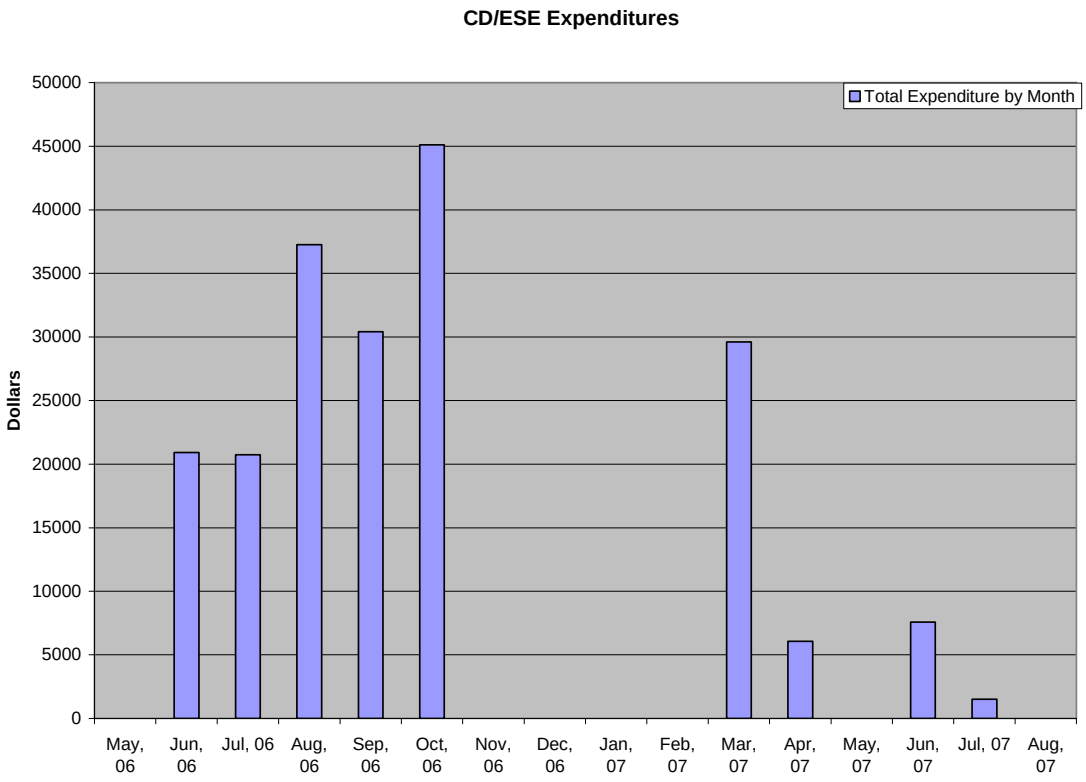


Figure 2
CD/ESE Expenditure by Month

It should be noted that a significant additional effort not charged to LANL was required to complete this work. For example, Marcos Turqueti never charged against the PHENIX budget code (according to the effort reports). He was, however, a significant contributor, without whose efforts, the project would never have been completed. The effort was contributed by ESE because of its synergy with other pixel projects at Fermilab.

It should also be noted that during the period between November, 2006 and February 2007, there were no charges issued against the PHENIX code. It was during this time that PHENIX funds for the initial SOW had been exhausted. It was not until February, 2007 that additional funds were made available as a result of the extended SOW. Effort was reported for February, 2007 but the charges for that effort did not get logged until the following month. The initial SOW was written for a total of $150,108 to cover a period between March, 2006 and November, 2007. When funding for the initial SOW was consumed, the extension was negotiated for an additional $50,000. These two agreements made a total of $200, 108 available for charges by ESE. The project was closed out having consumed a total of $199,194.17 in charges. The funds for the Statement of Work and the subsequent modification were effectively exhausted at the end of July 2007 and the budget code was closed out for August, 2007.

Documentation:

Hardware Design Documentation:

The following hardware design documents may be found in the PPD Experimentation Physics Projects (EPP) online document database:

Document Number EPP-doc-304-V1 contains schematics, layout, and Bill of Materials (BOM) for the the KISS HDI V1 Portcard.

The KISS HDI V1 Portcard schematics may also be found in the Computing Division Database (document number CD-doc-2393-v1).

The KISS HDI V1 Portcard layout may also be found in the Computing Division Database (document number CD-doc- 2394 -v1).

The KISS HDI V1 Portcard Bill of Materials (BOM) may also be found in the Computing Division Database (document number CD-doc-2395-v1).

Document Number EPP-doc-328-V4 contains schematics, layout, and Bill of Materials (BOM) for the Pixel Plane PCB. A detailed specifications document is also available at that site.

The Pixel Plane PCB schematics may also be found in the Computing Division Database (document number CD-doc-2396-v1).

The Pixel Plane PCB layout may also be found in the Computing Division Database (document number CD-doc-2397-v1).

The Pixel Plane PCB BOM may also be found in the Computing Division Database (document number CD-doc-2398-v1).

Also available is the Pixel Plane Specification authored by ESE members. This document is available in the Computing Division Database (document number CD-doc-2399-v1).

Firmware Documentation:

Documentation to support the test stand software is available online at the following website:

http://www-ese.fnal.gov/Phenix/index.html

At this site, links are provided that support downloading of ZIP archives with the firmware for the test stand FPGA. The firmware has been developed for the PCI Test Adapter, Version 2 (PTA2) test stand hardware. A number of archived versions are available as well as the most current version.

Software Documentation:

Documentation to support the test stand software is available online at the following website:

http://www-ese.fnal.gov/Phenix/index.html

At this site, links are provided that support downloading of the software and online help pages for users to consult. A number of archived versions are available as well as the most current version.

Fabrication Charges:

Item	Task Code	Cost	Vendor
KISS HDI Port Cards	18.2.16.1.3.3	$2050	Metro Circuits
Kiss HDI V1	18.2.16.1.3.3	$6148.75	MicroConnex
Pixel Plane Components	18.2.16.1.3.3	$433	Various

The Pixel Plane PCB, version 2 of the KISS HDI, and most of the other parts were purchased by LANL.

Lessons Learned:

Testing revealed a design flaw when using the Micrel SY89828L clock distribution device. The device does not reliably support having the multiple outputs being wired together. During bench testing, the devices were being damaged apparently because the two outputs can be simultaneously enabled for a brief period of time.

The resolution to this problem is to replace the Micrel SY89828L clock distribution device with the Maxim MAX9153 clock driver. This modification will require a schematic and layout change to be made to the prototype design. An alternative approach to modifying the schematic and layout would be to design a mini-board that can support the Maxim MAX9153 clock driver and be wire bonded to the pads that already exist for the Micrel SY89828L device. While not the neatest solution, this would make the existing prototype pixel plane useable as a production design without modification to the plane itself.

Successful implementation of either of the above solutions will produce a pixel plane which resolves all known issues as of Sept. 1, 2007.

Additional Factors:

It should be noted that ESE performed a great deal of work that did not fall under the requirements as described in the statements of work. These activities included:

1. The design of the KISS HDIs.
2. The automation of a wafer probe test stand in Wilson Hall to support testing of entire FPIX2.1 readout chip wafers.
3. Investigations into the nature of stability problems with the FPIX2.1 readout chip.

All of these tasks were time consuming and required the expertise of engineers in ESE to successfully perform them. In addition, items 2 and 3 in this list required ESE engineers to develop additional test stands with PTA2 boards that were loaned from the ESE pool.

There were also delays in the completion of mechanical details that impacted the delivery of the final pixel plane PCB. In some cases, modifications to mechanical details resulted in the need for previously completed sections of the layout to be re-rerouted.

The delivery of some electronics products was delayed as a result of quality issues with some of the vendors. The HDIs were initially to be fabricated by DyConnex. However, other customers were given priority and another customer, MicroConnex was eventually retained for the work. This vendor had to go through several iterations (and substantial delays) before the entire order of 25 units was completed. While the production of HDIs is considered a challenging technology, the delays that resulted were in excess of what was expected. As of Sept. 1, 2007, a second order for HDIs (including modifications as a result of lesson learned in lab tests) has been provided by DyConnex. These HDIs appear to be good quality although, as of the writing of this report, no testing has been done.

In addition, the Port Cards (fabricated by MetroCircuits) were also delayed as multiple fabrication cycles were needed to produce the boards with suitable quality.

Finally, two fabrication runs from King Circuits were needed to complete the order for Pixel Plane PCBs.

Project Work Breakdown Schedule (WBS)

The following figure illustrates the final version of the WBS for the project.

ID	WBS	Task Name	% Complete	Duration	Start
1	**1**	**FNAL/CD PHENIX**	**100%**	**388 days**	**3/1/06**
2	1.1	Funds from LANL received at FNAL/CD	100%	0 days	3/1/06
3	1.2	Funds for extension	100%	1 day	2/1/07
4	**1.3**	**Pixel Plane - Prototype**	**100%**	**139 days**	**2/2/07**
5	1.3.1	Schematic entry	100%	30 days	2/2/07
6	1.3.2	Simulations	100%	12 days	3/16/07
7	1.3.3	Develop mechanical requirements with mechanical team	100%	18 days	4/3/07
8	1.3.4	Layout	100%	24 days	4/27/07
9	1.3.5	Pixel plane PCB delivered to FNAL	100%	55 days	5/31/07
10	1.3.6	Pixel plane PCB approved and delivered to LANL [to PPD]	100%	0 days	6/13/07
11	**1.4**	**PM test board**	**100%**	**52 days**	**5/24/06**
12	1.4.1	Schematic entry	100%	12 days	5/24/06
13	1.4.2	Simulations	100%	6 days	6/9/06
14	1.4.3	Develop mechanical requirements with mechanical team	100%	6 days	6/19/06
15	1.4.4	Layout	100%	18 days	6/27/06
16	1.4.5	PM test board delivered to FNAL	100%	10 days	7/21/06
17	1.4.6	PM test board approved and delivered to LANL	100%	0 days	8/3/06
18	**1.5**	**Pixel plane PCB - Production**	**100%**	**52 days**	**6/13/07**
19	1.5.1	Received sytem and pixel plane PCB mechanical requirem	100%	0 days	6/13/07
20	1.5.2	Schematic entry	100%	15 days	6/14/07
21	1.5.3	Simulations	100%	6 days	7/5/07
22	1.5.4	Develop mechanical requirements with mechanical team	100%	10 days	7/13/07
23	1.5.5	Layout	100%	20 days	7/27/07
24	1.5.6	Pixel plane PCB delivered to FNAL	100%	1 day	8/24/07
25	1.5.7	Pixel plane PCB approved and delivered to LANL	100%	0 days	8/24/07
26	**1.6**	**Test stand**	**100%**	**197 days**	**3/1/06**

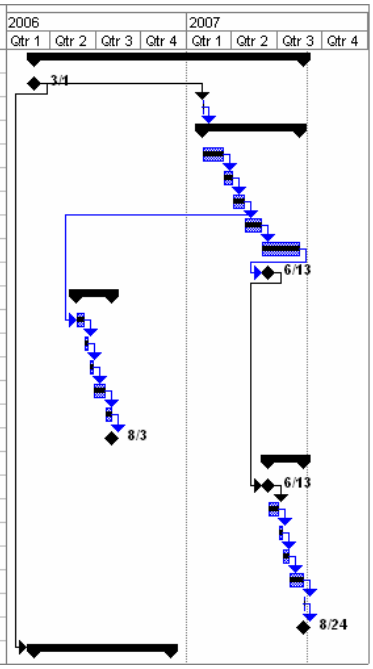
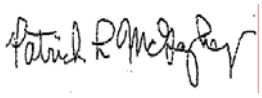


Figure 3
Project WBS

Concurrences:



10/4/07

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Date

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