

COUPP CAMERA TRIGGER INTERFACE CONTROLLER / CAMERA LED INTERFACE MODULE (CTIC/CLIM) USER MANUAL

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1 INTRODUCTION

This document describes the information necessary for users to operate the COUPP Camera Trigger Interface Controller (CTIC) module, and its companion Camera LED Interface Module (CLIM).

2 THEORY OF OPERATION

2.1 CTIC MODULE

The CTIC module provides the following functions:

- Controls the frame rate and synchronization of the cameras.
- Accepts triggers from all trigger sources, and fans them out to all trigger destinations synchronously.
- Provides the COMPRESS signal to the system PLC.
- Provides power to the cameras.
- Controls the timing and duration of LED backlight Flash Enable signal.
- Provides a diagnostic logic analyzer port.
- Provides a subset of signals to an I/O card in the host PC.

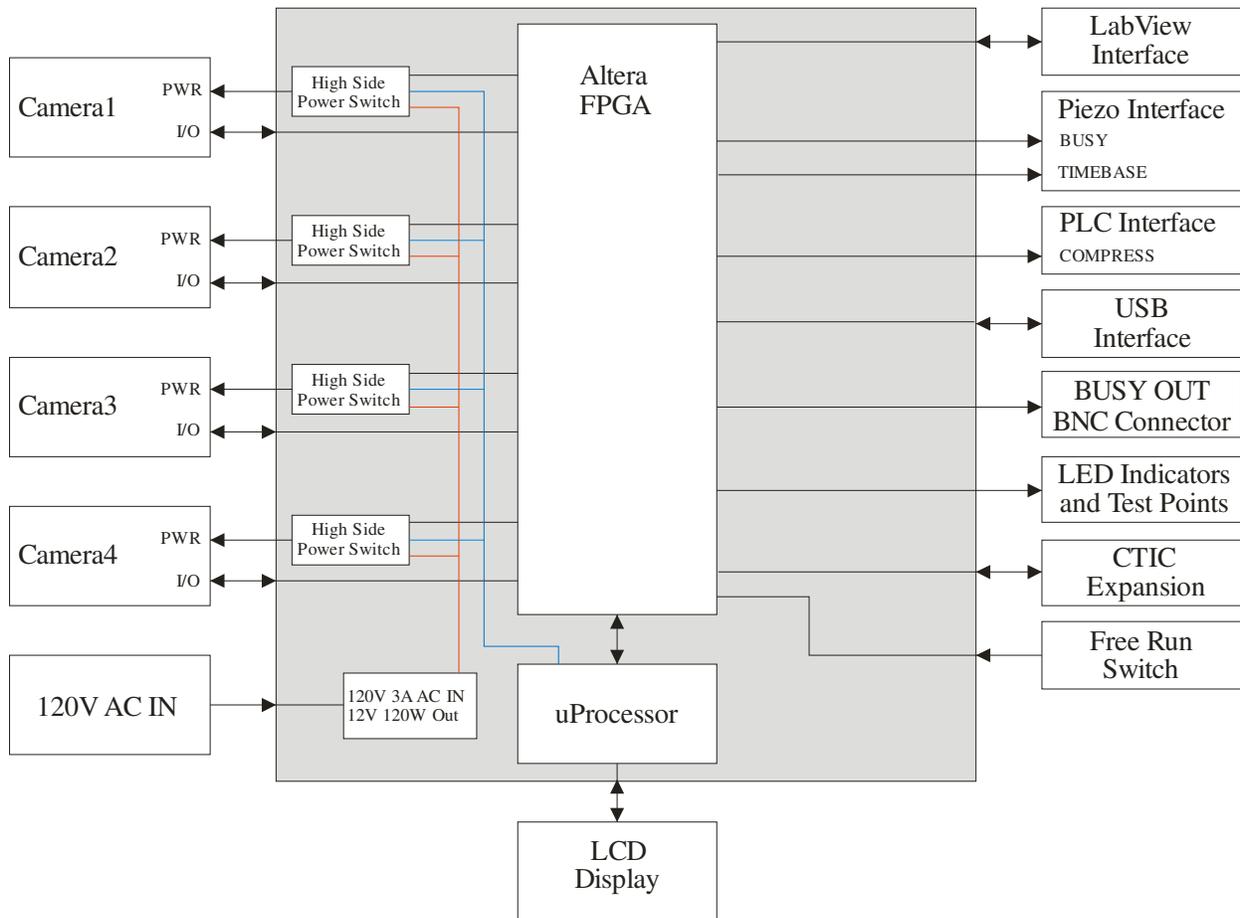


Figure 1 CTIC Block Diagram

2.1.1 CTIC FUNCTIONAL BLOCKS

2.1.1.1 Altera FPGA

The Altera CycloneIII FPGA is the heart of the CTIC module. The FPGA controls the various functions listed below:

- Controls power to the installed cameras.
- Provides triggers to installed cameras.
- Provides triggers to LED flash unit.
- Interfaces to the PLC controller.
- Interfaces to the Piezo controller.
- Interfaces to Linux PC running LabView.
- Interfaces to Linux PC via a USB port.

All of the above functions are configured by the USB interface to the Linux PC. The command protocols for the USB port is explained elsewhere in this document.

2.1.1.2 ARM7 Microcontroller

The CTIC uses an ARM7 LPC2468 microcontroller from NXP Semiconductor. Presently the LPC2468 is used to monitor the camera voltages and currents and display them on an LCD display. The LPC2468 and LCD display will mostly be used during the CTIC system debugging and may not be in the final production units unless it is deemed useful.

2.1.1.3 USB Port

The USB 2.0 port is used by the CTIC to communicate with the host Linux PC. The port will show up in the Linux PC as two COMM ports. One port is used to configure and communicate with the CTIC. The other port is used to access the camera's serial console ports.

2.1.1.4 Camera Interface Ports

The CTIC can support up to four cameras. There are two connections from the CTIC to each camera, a power and an I/O cable. The power cable supplies 12V DC @ 2Amps max to the camera and has the camera's RS232 console signals. The power connector is a 10pin Hirose connector (part number: HR10A-10P-10S). The I/O cable gives the CTIC access to the camera's programmable input and output ports. These I/O pins will be used for camera triggers and status. The CTIC will convert the camera I/O logic levels into levels that the FPGA can interface with. The I/O connector is a 12pin Hirose connector (part number: HR10A-12P-10S).

2.1.1.5 LED Flash Interface

The CTIC has a Flash output connector for each camera that connects the CTIC to the LED Flash unit. Up to four independent CLIM modules can be driven, but typically only one will be used. The flash trigger signal is a 5V TTL signal that can drive 50 ohms.

2.1.1.6 LabView Interface

The LabView interface consists of 16 programmable 5V I/O lines that connect back to the host computer's PXI-6221 data acquisition card. These lines will be used to enable and disable the CTIC, and to provide triggers and status back to the Linux PC running LabView. The CTIC will convert the 5V TTL level signals into levels that the FPGA can interface to. The LabView connector will be a 10pin circular Cannon connector (part number xxxx).

2.1.1.7 Piezo Interface

The Piezo interface consists of two BNC connectors. The 1st BNC connector is a "BUSY" signal that tells the Piezo unit that the system is currently in a busy state. The 2nd BNC provides a time base to the scope module that is digitizing the output of the Piezo sensor. Both BNC's use 5V TTL signals that can drive 50 ohms.

2.1.1.8 PLC Interface

The PLC interface is used to tell the PLC to start a compress cycle. The CTIC uses a relay to short two pins on the PLC's connector to initiate a compress cycle. When the Normally Closed relay is energized, the pins are not shorted, and the PLC can cycle the chamber into superheat mode. When the relay is de-energized, the contacts are closed, signaling the PLC to start a compress cycle. Failure of the relay will force the PLC into compress mode. The PLC connector is a 4pin Cannon circular connector (part number xxxx).

2.1.1.9 Busy Out

The ‘Busy Out’ BNC connector is a general purpose output used to tell any connected device that the CTIC is currently in a “Busy” state. The Busy BNC uses a 5V TTL signal that can drive 50 ohms.

2.1.1.10 LED indicators and test points.

The CTIC will have the following LED’s on its front panel:

- Power LED
- Free Run LED
- Busy LED
- Compress LED
- Camera 1-4 Power LED’s
- Camera 1-4 Trigger LED’s
- Camera 1-4 Shutter active LED’s
- Camera 1-4 Event LED’s
- Camera 1-4 Flash LED’s

The test points will allow easy access to various CTIC signals and voltages that will help speed up the debugging of a system. Using the LA Select rotary switch on the front panel, one of eight different diagnostic signal sets can be selected.

2.1.1.11 CTIC Expansion Port

The CTIC Expansion port is used to connect two CTIC’s together to control 8 cameras. The expansion port connector is a 20pin circular Cannon connector (part number xxxx).

2.1.1.12 Free Run Switch

The free run switch will put the CTIC in a “Free Run Mode”. When in “Free Run Mode” the CTIC will trigger the cameras without being connected to the host Linux PC. This mode can be overridden by the Linux PC’s USB port or the LabView interface.

2.1.1.13 LCD Display

The LCD display is by the microprocessor to display status for the installed cameras. Currently the microprocessor will monitor camera voltage and current.

2.1.1.14 Frame Rate Control

Cameras will be programmed to acquire a video frame upon receipt of a Frame Enable signal from the CTIC module. The Frame Enable signal to each camera is independently controllable through configuration registers in the CTIC module. The Frame Enable signal therefore controls the frame rate and timing of the camera(s). The Frame Enable logic is driven by a clock with a 1 us period. All camera frame timing is configurable to a 1 us resolution.

To set the frame rate, the Frame Timer Register is loaded with the frame period in microseconds. The frame timer counter is reset to zero, then increments by one count every microsecond. The incrementing timer count wraps to zero when the frame period count is reached. All camera and flash timing is based on the Frame Timer.

Once the Frame Timer Register is configured, the frame timing of each camera can be set relative to each other by writing to the Frame Count register for the desired camera. This selects the Frame Timer count value that the camera will acquire a frame on. Valid values for the Frame Count Register are 0 through the value set in the Frame Timer Register. If a value larger than that loaded into the Frame Timer Register is loaded into the Frame Count Register, the camera will never receive a Frame Enable signal. This arrangement allows the frame timing of individual cameras to be configured to acquire frames independently at different times. Note that all cameras acquire at the same frame rate, but they can be configured to acquire at different times relative to each other. Cameras are set to acquire at the same time by setting their Frame Timer Registers to the same value.

2.1.1.15 Flash Control

The LED backlights are enabled by a CTIC output. The timing of this output is controlled by the Flash Timing Register. This 32-bit register contains the delay and duration of the LED flash relative to the Frame Enable signal for each camera. Delay and duration values are in microseconds. The delay value specifies the number of microseconds to delay before enabling the LEDs after the Frame Enable signal is sent to the cameras. The duration value is the number of microseconds that the LED remains on before turning off.

2.1.1.16 Trigger Fanout

Upon receipt of a trigger from any of the trigger sources, the trigger is synchronized to the 1 MHz CTIC control clock, and then output to all trigger destinations on the next clock cycle. Triggers are driven true for one clock cycle then negated. Trigger sources include the cameras, the host PC, the Piezo system, and the front panel External Trigger Input connector. Trigger destinations include the cameras, the host PC, the PLC, and the front panel Trigger Output connector.

2.1.2 CONFIGURATION AND CONTROL

Configuration and control of the CTIC is done by writing to a memory mapped register set. This register set is accessible via the USB connection or by the embedded ARM Microcontroller.

2.1.2.1 USB Communication

When connected to a host PC through USB, the CTIC appears as two USB Virtual Comm Ports (VCPs). One VCP appears as an FTDI FT232R device, and the second VCP appears as an FTDI FT245B device.

2.1.2.1.1 FT232R VCP

The FT232R VCP is used to connect to one of the four serial consol port interfaces of the four cameras or the consol port of the CTIC's ARM microcontroller. One of the five consol ports can be selected using the FT232R's CBUS pins, CBUS0 through CBUS3. On reset, the default consol port is that of the CTIC's ARM Microcontroller. To select one of the four camera consol ports, set the CBUS pins as follows:

<i>FT232R CBUS Address (CBUS3 – CBUS0)</i>	<i>Consol Port Selected</i>
0b0xxx	CTIC ARM Microcontroller
0b1000	Camera 0 Consol Port
0b1001	Camera 1 Consol Port
0b1010	Camera 2 Consol Port
0b1011	Camera 3 Consol Port

Refer to the FT232R data sheet (FTDI Document No.: FT_000053) for details on programming the CBUS pins.

2.1.2.1.2 FT245B VCP

The FT245B VCP communicates with the CTIC's configuration and control register set in the FPGA. Note that this register block can also be accessed by the CTIC's ARM microcontroller (See: Register Map in this document).

Writing and reading configuration registers through the VCP is done with ASCII characters in the same fashion as any comm port. The CTIC always responds with a command response string when a command string is received. CTIC command and response strings are formatted as follows:

<i>start</i>	<i>header</i>	<i>address</i>	<i>payload3</i>	<i>payload2</i>	<i>payload1</i>	<i>payload0</i>	<i>checksum</i>	<i>end</i>
@	AA	BB	CC	DD	EE	FF	GG	!

Where:

Start = ASCII 0x40 "@"

Header (AA) = (8-bits) Command on write to CTIC. Status on reply from CTIC.

Valid commands: Null 0x00, Read Register 0x01, Write Register 0x02

Valid status responses: Command Accepted: 0x00, Command Error: 0x01

Address (BB) = (8-bits) CTIC Register address

Payload (CCDDEEFF) = (32-bits) Register data

Checksum (GG) = (8-bits) Truncated, unsigned running addition of header, address, and payload bytes

End = ASCII 0x21 "!"

Example 1:

Read register at CTIC register address 0x01:

Command string sent to CTIC: @01010000000002!

Where the leading 01 signifies a register read command, the following 01 is the register address, and the trailing 02 is the checksum. Note that since this is a read command, the payload bytes are ignored, except for generation and checking of the checksum. Upon receipt of this command, the CTIC will transmit a response:

Response from CTIC: @0001DDDDDDDDCC!

Where the leading 00 signifies a successful operation. The following 01 is the register address echoed, DDDDDDDD is the 32-bit hex value of the contents of CTIC control register 0x01, and CC is the checksum.

Example 2:

Write 0x12345678 to register at CTIC address 0x01:

Command string sent to CTIC: @0204123456781A!

Where the leading 02 signifies a register write command, the following 04 is the address of the register to write to, 12345678 is the 32-bit data to write, and 1A is the checksum.

Upon receipt of this command, 0x12345678 will be written into the register at CTIC address 0x04, and the CTIC will transmit a response:

Response from CTIC: @00041234567828!

Where the leading 00 signifies a successful operation, 04 is the address echoed, 12345678 is the data echoed, and 28 is the checksum.

Example 3:

Send an errant command to CTIC:

Command string sent to CTIC: @01020304!

This command is malformed. Start and end characters are correct, but an incorrect number of payload bytes is an error.

Upon receipt of this command, the CTIC will ignore it, but generate a response:

Response from CTIC: @01000000000001!

Where the leading 01 indicates an unsuccessful operation, the 10 zeros following are meaningless, and the trailing 01 is the checksum.

2.1.3 REGISTER MAP

USB Address	Microcontroller Address	Function
0x00	0x00000	CSR
0x01	0x00004	Camera Control
0x02	0x00008	CTIC Control
0x03	0x0000C	Frame Timer Register
0x04	0x00010	Camera 0 Frame Count
0x05	0x00014	Camera 1 Frame Count
0x06	0x00018	Camera 2 Frame Count

0x07	0x0001C	Camera 3 Frame Count
0x08	0x00020	Flash Control
0x09	0x00024	Flash Timing
0x0A – 0xFD	0x00028 – 0xFFFF7	Reserved
0xFE	0xFFFF8	Camera Power Enable
0xFF	0xFFFFC	Firmware Version

0x00 (0x00000) CSR Register

31	2	1	0
Reserved		Busy Clear	Global Enable

Bit 31 – 2 Reserved. These bits are unused by the CTIC module.

Bit 1 Busy Clear. Setting this bit clears the Busy output of the CTIC. Busy is set true by an event trigger generated by any of the trigger sources.

Bit 0 Global Enable. When 0 the CTIC camera and flash control signals are held negated. When 1, CTIC camera and flash control signals are generated as per CTIC configuration registers.

0x01 (0x00004) Camera Control Register

31	8	7 – 4	3 – 0
Reserved		Manual Event Trigger	Camera Enables

Bit 31 – 8 Reserved. These bits are unused by the CTIC module.

Bit 7 – 4 Manual Event Trigger. Setting one of these bits high forces the corresponding camera to generate a trigger. Bits 7 – 4 map to cameras 3 – 0.

Bit 3 – 0 Camera Enables. When one of these bits is set high, the corresponding camera Frame Enable and Flash signals are generated as per CTIC configuration registers. When one of these bits is low, the corresponding camera Frame Enable and Flash signals are held negated.

0x02 (0x00008) CTIC Control Register

31	0
Reserved	

This register is currently unused.

0x03 (0x0000C) Frame Timer Register

31	20	19	0
Reserved		Camera Frame Rate Cycle Time (in microseconds)	

Bit 31 – 20 Reserved. These bits are unused by the CTIC module.

Bit 19 – 0 (Hex) Camera Frame Rate Cycle Time. The value in this register is used by the Camera Frame Timer to set the camera frame rate. Write the camera frame cycle time in microseconds to this register to set the camera frame rate. Note that frame rates of more than 180fps (cycle time values of less than 0x15B4) are not supported, and will cause undefined behavior in the cameras. The minimum frame rate supported is 0.9537 frames per second (one frame every 1.049 seconds).

0x04 (0x00010) Camera 0 Frame Count Register

31	20	19	0
Reserved		Camera 0 Frame Acquire Count	

Bit 31 – 20 Reserved. These bits are unused by the CTIC module.

Bit 19 – 0 Camera 0 Frame Acquire Count. When the Camera Frame Timer reaches the value in this register, Camera 0's Frame Acquire signal is driven true for 1 microsecond, causing the camera to acquire a video frame.

Valid values for the Frame Acquire Count Registers are any value between 0 and the value in the Camera Frame Rate Cycle Time Register, inclusive. If a Frame Acquire Count Register is loaded with a value higher than that in the Camera Frame Rate Cycle Time Register, the camera's Frame Acquire signal will never assert true. This condition will effectively disable the camera.

Each of the four cameras has its own Camera Frame Acquire Count Register, allowing camera frame acquisition between cameras to be synchronized or staggered. Setting the Camera Acquire Count values for the different cameras identically will cause the cameras to acquire at the same time. To stagger frame acquisition times for different cameras, set the Frame Acquire Count differently for the different cameras. The Camera Frame Timer increments by one count each microsecond, so if Camera 0 is set to acquire at count 0, and Camera 1 is set to acquire at count 10, then the relative time between the two cameras frame acquisitions will be 10 microseconds.

0x05 (0x00014) Camera 1 Frame Count Register

31	20	19	0
Reserved		Camera 1 Frame Acquire Count	

Function similar to that of Camera 0 Frame Count Register.

0x06 (0x00018) Camera 2 Frame Count Register

31	20	19	0
Reserved		Camera 2 Frame Acquire Count	

Function similar to that of Camera 0 Frame Count Register.

0x07 (0x0001C) Camera 3 Frame Count Register

31	20	19	0
Reserved		Camera 3 Frame Acquire Count	

Function similar to that of Camera 0 Frame Count Register.

0x08 (0x00020) Flash Control Register

31	4	3 - 0
Reserved		Flash Enables

Bit 31 – 4 Reserved. These bits are unused by the CTIC.

Bit 3 – 0 Flash Output Enables. When set to a one, the corresponding Flash Enable output is enabled. When set to a zero, the corresponding Flash Enable output is disabled.

0x09 (0x00024) Flash Timing Register

31	25	24	16	15	9	8	0
Reserved		Flash Delay Value		Reserved		Flash Duration Value	

Bit 31 – 25 Reserved. These bits are unused by the CTIC.

Bit 24 – 16 Flash Delay Value (Hex). Value defines the delay time in microseconds between the Frame Enable signal going true, and the LED Flash Enable outputs going true.

Bit 15 – 9 Reserved. These bits are unused by the CTIC.

Bit 8 – 0 Flash Duration Value (Hex). Value defines the duration the LED Flash Enable signal stays true once set, in microseconds. After the defined time expires, the LED Flash Enable signal goes false.

0xFE (0xFFFF8) Camera Power Enable Register

31	4	3 – 0
Reserved		Camera Power Enables

Bit 31 – 4 Reserved. These bits are unused by the CTIC.

Bit 3 – 0 Camera Power Enables. When high, the corresponding camera power supply is turned on. When low, the corresponding camera power supply is turned off.

0xFF (0xFFFFC) CTIC Firmware Version Register

31	24	23	16	15	8	7	0
Minor Version Number		Month		Day		Year	

Bit 31 – 24 Minor Version Number (BCD). Serial version number of code generated on the day identified (larger number is newest).

Bit 23 – 16 Month (BCD). Decimal month of day code was generated.

Bit 15 – 8 Day (BCD). Decimal day of month that code was generated.

Bit 7 – 0 Year (BCD). Decimal least significant digits of year that code was generated (all years 21st century).

2.2 CLIM MODULE

The CLIM Module provides the following functions:

- Provides power for back-light LED array.
- Provides over-current protected drivers for 8 arrays of 10 Luxeon LXHL-LD3C high intensity Red LEDs. The 10 LEDs in each array are arranged in two parallel strings of 5 LEDs.
- Monitors and displays current draw on all LED strings.
- Accepts LED On signal from CTIC module.

- Provides stand-alone LED testing capability.

2.2.1 CLIM FUNCTIONAL BLOCKS

2.2.2 CLIM FRONT PANEL

2.2.3 CLIM BACK PANEL

3 MECHANICAL SPECIFICATIONS

3.1 FRONT PANEL CONTROLS AND INDICATORS

3.2 BACK PANEL CONNECTORS

3.3 PHYSICAL

The CTIC and CLIM are both 3U, 19" rack mounted, 35mm deep modules.

4 POWER AND COOLING REQUIREMENTS

Air cooled. 110VAC.